Supercapacitor based on porous structure of AAO template

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Abstract

As a kind of energy storage devices, supercapacitor has a broad application prospect in using renewable energy, powering electric vehicles, enabling portable equipment, and cordless powering internet of thing. This thesis report the research on the development of on-chip MEMS supercapacitors.

We focus on both electrostatic capacitor and electrochemical capacitors. We try to improve the energy density and power density of these capacitors by different methods.

A. Electrostatic supercapacitor.
   1. In order to increase the effective area for increased capacitance, we use (anodic aluminum oxide (AAO) template as the scaffold for electrode of the capacitors, which has high pore density, thus the high specific area. Gold or copper was deposited as the electrical conducting layer. For the dielectric layer, we can deposit SiO2 or HfO2 by sputtering or atomic layer deposition (ALD technology).
   2. To further improve energy density, a multilayer capacitor design has been proposed. The layers of the electrode and dielectric in sequence can fabricated on the AAO template by such as ALD or sputtering technology. Formed static capacitors in parallel connection will greatly increase the capacitance.

B. Electrochemical supercapacitor.
   Based on the AAO scaffold, we fabricated an electric double layer capacitor (EDLC) using gold layer as the active electrode layer. To improve the energy density of EDLC, unsymmetrical design consisting of EDLC electrode and pseudo electrode is investigated. MnO2 is employed as the pseudo material which we can load it on the AAO template by electrochemical plating method.

Profiler meter, probe station, and Zahner IM6 Electrochemical workstation were utilized to characterize the sample structure such as the thickness of the electrical conducting and dielectric layer, the conductivity of the conducting layer, and capacitors performance. According to the result, we have achieved the specific capacitance about 1-2uF/cm2 for electrostatic supercapacitor fabricated by sputtering process, which is smaller than the published results (about 10-100uF/cm2) from capacitors fabricated by ALD process. The specific capacitance of EDLC and pseudo supercapacitor with porous structure has an significant improvement compare with the flat one. We achieved the specific capacitance about 50-100mF/cm2 for pseudo supercapacitance.
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CHAPTER 1: INTRODUCTION

1.1 The background of energy storage device

In response to the changing of global landscape, energy has become a primary focus of the major countries and research community. There has been great interest in developing and more efficient energy storage devices. The supercapacitor is one electrochemical energy storage device that holds promise to promote major advances in energy storage field.

Supercapacitors, also known as ultracapacitors or electrochemical capacitors, is a new type of energy storage device which utilize high surface area electrode materials and thin electrolytic dielectrics to achieve capacitances several orders of magnitude larger than conventional capacitors[1]. The power density is between capacitor and battery. The supercapacitor possesses high power density, a long cycle life, and high cycle efficiency, has attracted more and more attention owing to its wide range of potential applications, such as hybrid power sources for electric vehicles, and pulse laser technique. In some of the applications, supercapacitors can serve as a short-time energy storage device with high power capability and allow for storing the energy from regenerative braking[2]. Therefore, it not only stores energy but also can save a lot energy from the waste energy[3].

1.2 Classification of supercapacitor

According to the different working principle, we can divide the supercapacitor into Micro/Nano electrostatic supercapacitor and electrochemical capacitor. Moreover, electrochemical capacitor can be divided into three type’s capacitors such as electric double layer capacitors, pseudocapacitors and hybrid capacitors. As the EDL supercapacitor, which store electric energy into Helmholtz double layer at the interface between electrode and electrolyte. Pseudocapacitors, by contrast, achieve energy storage with redox reaction with the charge transfer between electrode and electrolyte. The typical electrode materials for pseudocapacitors are metal oxides (e.g. ruthenium oxide, manganese oxide that we will use in this thesis) and conducting polymers. However, there still have disadvantage in EDL capacitors and pseudocapacitors for practical applications because of the low capacitance in EDL capacitors and stability problem in pseudocapacitors. Thus, hybrid devices with composites of carbon material and pseudocapacitive additive were investigated to combine the two energy storage mechanisms[4][5].

1.3 Working principle of supercapacitor

a. Micro/Nano electrostatic capacitor mainly composed by electrostatic interaction
induced the electron moving between metal electrodes and the dielectric layer, through the movement of the electrons complete the energy storage and release. If all the electrostatic capacitors were fabricated on the Micro/Nano structure. We call this capacitor as M/N electrostatic supercapacitor. This working principle is almost the same with conventional capacitors consist of two conducting electrodes separated by an insulating dielectric material. The Micro/Nano structure just used for increasing the effective area in the capacitor. When a voltage is applied to a capacitor, opposite charges accumulate on the surfaces of each electrode. The charges are kept separate by the dielectric, thus producing an electric field that allows the capacitor to store energy.

According to the principle of electrostatic capacitor energy storage. The calculation formula of the capacitor capacitance $C$ and the voltage $U$ between the sides as follow (1-1) (1-2). From the formula, we can see. Capacitance $C$ is proportional to the electrode area and inversely proportional to the thickness of dielectric layer. The voltage $U$ is proportional to the breakdown field strength and inversely proportional to the dielectric layer thickness $d$.

$$C = \frac{\varepsilon_0 \varepsilon_r S}{d} \quad (1-1)$$
$$U = E d \quad (1-2)$$

$\varepsilon_0$, Vacuum dielectric constant. $\varepsilon_r$, relative dielectric constant of the dielectric layer.[4] $d$ is the thickness of the dielectric layer. $A$ is the effective contact area between electrodes and the dielectric layer. $E$ is the breakdown field strength of the dielectric layer. From the formulas we can see. If we want to improve the capacitance $C$, we must decrease of the dielectric layer thickness or increase the electrode area. Basic on this principle we have several different design, but all off them must be follow the principle so we use choose the high aspect ratio as my basic blueprint[5].

![Figure1- 1: Diagram showing the charge distribution in an electric double-layer capacitor when it is charged (left) and discharged (right)](image)
Double Electric Layer Capacitor (EDLC). Electric double layer capacitor is mainly composed of anode, electrolyte, and distance sleeve, which stores energy through the separation of electronic and ionic charges at the interface between electrode and an electrolyte solution. The mechanism of electric double layer supercapacitor was similar with the traditional electric capacitor. Essentially, all of them were product capacitance by static adsorption. The basic model of this capacitor was show in schematic Figure 1-2. Charge power was supplied by the external power source. When the phase of solid and liquid contact with each other. There will product confrontation electric charge layer which was negative and positive in the interface. There, the electric double layer we can regard as a parallel-plate condenser. One is made by material layer, and the other electrode was electrolyte ion layer. So the supercapacitor device we can regard as two double layer capacitor in series. For an electric double layer supercapacitor the distance between two electrodes was only several angstroms. So the capacitance will have a great increase because of the small distance. Electric double layer capacitor consist of two electrodes. Infuse electrolyte between the two electrodes and fully infiltrates. There have a diaphragm between the electrodes. In order to prevent electrodes and provide the channels for electrolyte ion migration. When charging, electron on the surface of the anode transfer out via the external circuit to cathode and gathered in the cathode. The potential of anode rise, in reverse, the potential in cathode decrease. The electron in internal electrolyte adsorbed to anode and cathode electrode surface followed the principle of electrical. Charge on the surface of two electrodes Gathered until saturated. Potential difference was increased. After change, the external electric field was disappeared. Ions was adsorbed on the anode surface. Positive ion was adsorbed on the surface of cathode. Electrostatic force made the charge ranged closely. The electric double layer was stable. When discharged. The electron in the cathode go back anode via external circuit. The electrical potential was disappeared during charging process. The ions come from electrolyte go back to solution. So the double layer capacitor was disappeared during this process. In the whole process. There have no Faraday electrochemical reaction. Just the physical adsorption and migration of electron during this process. So we know during this process, the distance between two electrode have no big difference. If we want to improve the capacitance, we must increase the superficial area of the electrode. So store more charge and improve the capacitance, we should try to improve the effective specific surface area. So, the AAO substrate with high specific surface area was a good choose for making supercapacitor.

An electric double layer capacitor offers higher capacitance and higher energy density than the normal electrolytic capacitor. Electric double layer capacitors are suitable for a wide range of applications, including memory backup in electronic devices, battery load leveling in mobile devices, energy harvesting, energy regeneration in automobiles, and more. A further increase in energy density, improved charge/discharge characteristics and thermal characteristics, as well as electrode material improvements are some of the technical challenges that still need to be addressed. The main characteristics of electric double layer capacitors are described below.

Capacitance: The surface structure of the activated carbon (pore diameter and volume, specific surface area) has a large influence on capacitance.
Internal resistance: An electric double layer capacitor can be considered an equivalent circuit where a large number of miniature capacitors having internal resistance are connected in parallel. The resistance component of the electrolyte and electrodes etc. creates the internal resistance which causes a drop in effective voltage. For large current discharge applications, internal resistance should therefore be kept as low as possible.

Leakage current: When an electric double layer capacitor is charged for an extended period of time, the charge current decreases but it does not become zero. Rather it settles at a certain constant value, which is called the leakage current. The magnitude of this current is determined by factors such as electrode material, cell construction, usage temperature etc.[7].

c. Pseudocapacitance is the electrochemical storage of electricity in an electrochemical capacitor (Pseudocapacitor). After electric double layer capacitor[8]. People invented the faradaic capacitor, also called pseudo capacitor. That was on the electrode surface and bulk. We do the electrochemical owe potential deposition and deposited electrochemical materials on the structures. In this area will store energy due to the highly reversible chemical redox reaction. This reaction can be thought as a type of chemical reaction between cell reaction and double layer capacitor. Electrode active material transfer electron during Faraday reaction. This is similar to the battery charge and discharge reaction from the nature[9][10]. But from reaction kinetics, the charging and discharging process were different with the cell reaction and meet the requirements of the reaction of the capacitance characteristics. The electric potential is almost linear relationship with the charge on the electrode. So this phenomena was similar with electric double layer supercapacitors[11][12]. Essentially. The difference between Faraday capacitance and electric double layer capacitor was that whether there have a charge transfer between the electrode material and electrolyte. Faraday capacitance is not only on the surface of electrode, also generated in the electrode internal. The active material can transfer electron on the location which have a certain depth from the electrode surface. Greatly improving the utilization factor of electrode material. Because of its rapid response. Faraday reaction happened on the surface and internal was finished almost at the same time. There did not have the chemical reaction which can affect the reaction rate. Further improves the power density and specific capacity the electrode[13]. For making electrode of faraday capacitor requires high specific surface with good electrical conductivity. So the AAO substrate also can have a good match[14].

d. The principle of capacitor energy storage. Based on the mechanism of charge storage, the energy stored in the tiny electrostatic capacitor we can see in the formula (1-3)

\[ E = \frac{1}{2}CV^2 \quad (1-3) \]

\( V \) is the working voltage of capacitor, \( C \) is the capacitance. Obviously, increase \( C \) and \( V \) will let the capacitor store more energy

\[ P = \frac{E}{t} - I^2R \quad (1-4) \]

And the power of the capacitor which can calculate by the formula of (1- 4). In this
formula \( t \) is the discharge time and \( I \) is the output current. \( R \) is the equivalent series resistance of the capacitor. In order to improve the power of capacitor, the capacitor must have a small equivalent series resistance and faster discharge properties. The equivalent series resistance mainly depends on the electrode material itself. So high performance, high energy density and power density micro capacitor general requirements the substrate with the high integration, set small fluid resistance, big specific surface area, wide working temperature and higher breakdown voltage and so on[10].

1.4 The current research status on the supercapacitor

Since the 21st century, Due to the traditional storage energy limited and non-renewable fossil fuels. To seek the new "again Raw energy, green environmental protection, stable and efficient " energy as a development trend in the work. So, how to storage and utilization energy effectively becomes a significant research topic. The emerging of new materials and preparation technology which have the flexibility and diversity character provide a broad platform for the development of the high-performance energy storage devices. Lithium ion batteries, tantalum capacitor, aluminum electrolytic capacitors, ceramic capacitors, film capacitors, and electrochemical capacitors become a research hotspot in the field of energy storage and conversion.

Lithium ion battery has the advantages of high energy density, small self-discharge efficiency and compared with nimh batteries[15], nickel cadmium battery the environment pollution is small, but its power density is low. Also has the phenomenon such as prone to overshoot, short circuit. There is not very security must be have the special protection
circuit to prevent over charge and over discharge. At present, researchers are still working on the new materials and appropriate technology for this battery. Especially the polymer type of lithium ion battery. Using the simplified protection circuit can work, to a certain extent, it can improve the output power and reliability of the lithium ion battery. During the year of 2008, Yun-Hui Huang, Etc through the polypyrrole (PPy) instead of traditional lithium ion battery carbon and adhesive[16], used electrochemical sink and chemical polymerization preparation LiFePO4 as the Cathode, improved the electric capacity of capacitor and ratio performance significantly. The results illustrate that the PPy/C - LiFePO4 Battery under high rate showed excellent capacitance characteristic, withstand voltage can reach 4 V. This is due to the electric deposition process which can provide the good contact between particles and current collector.

As a storage element, compared with batteries, there is no limit on the current which can be instantaneous charge and discharge, we use capacitors as an element provide instantaneous pulse current for high power devices. Therefore, the researchers around the world are committed to new type of material development and the improvement of the manufacturing process. Among them, the tantalum capacitor also attract tremendous attention[17]. 1956 Bell first proposed solid tantalum electrolytic capacitor in the United States and it has the largest specific volumetric capacity during all products at that time. In figure1-2, it is the basic structure[12][18]. Solid tantalum electrolytic capacitor has the advantage such as high frequency characteristic, width temperature scope, and given a large specific storage volume, tantalum oxide thin film dielectric constant is higher than aluminum oxide film, so adapted to demand of the development in micro miniature electronic technology. But the price of tantalum capacitor is more expensive and easy to make the device produces "soft breakdown" phenomenon under the environment of high overload, and the electrode in the production and using will produce harmful substances, these factors all restrict the development of tantalum capacitor[19][20][21].

1.5 Research Motivations and Objectives

In order to overcome the major obstacles of supercapacitor research: the low energy density and high cost, improvement of current technologies are needed in the studies of fabrication porous structure. Find the suitable method for preparation substrate that can retain the ordered porous structure and the architecture for better capacitance performance. To realize that goal, an effective electrochemical etching routine of 3D substrate material, a new electrolyte with suitable bias voltage are critical aspects of the research were mentioned in this thesis. The general purpose of the research is to enhance the performance of supercapacitors, to reduce the cost and to miniaturize the size. The performance enhancement can be characterized as parameters such as specific capacitance, energy density, power density, and lifetime[17].

This thesis presents a two-step anodic oxidation route of AAO porous structures, also show a way to fabricate the Micro/Nano electrostatic supercapacitor that achieves capacitance 1-10uF/cm². Basing on this substrate, we also fabricate electric double layer supercapacitor
which achieves high EDL capacitance of 50-100mF/cm² which makes it suitable for high power applications. All the electrochemical measurement results were given in the electrolyte of 1mol/L sodium sulfate[22].

1.6 The organization of this thesis

This thesis is organized as the following.

In Chapter 2, we will discuss the on chip supercapacitor which involve the electrostatic supercapacitor based on Micro/Nano structure, and electrochemical supercapacitor based on electrochemical capacitance by EDLC and pseudo-capacitor.

In Chapter 3, Technology for on chip supercapacitor and the set up for experiment.
1. Micro/Nano scaffold fabrication based on aluminum foil.
2. Metal layer deposition based on the AAO substrate.
3. For the electrostatic capacitor, making the nano-holes-electrostatic supercapacitor based on AAO substrate.
4. For the electrochemical supercapacitor, we use C-V cycle method loading MnO₂ as the pseudo-capacitance material.
5. During these processes, we will use thermal evaporator machine, and sputtering AJA etc.

In Chapter 4, experiment part will detail description of the electrochemical etching, and multilayer deposition. In addition, the fabrication details and characterization results will be provided. Characterization involves multiple techniques like scanning electron microscopy (SEM), atomic force microscopy (AFM), and Energy Dispersive X-ray Detector (EDX) to represent the structures. Optimizing the fabrication parameters in AAO process and finding the relationship between power source and the depth of nano-holes by testing and characterization instruments. Finding the relationship between power source and the aperture size of nano-holes by testing and characterization instruments. Fabricating the AAO template as the substrate of capacitor based on this optimized parameters.

In Chapter 5, results and discussion. Using Zahner IM6 Electrochemical workstation test the impedance. C-V and impedance of all supercapacitor under different conditions. Electrochemical measurements are used to extract the specific capacitance, energy density, and power density, and comparing the result, we got from different samples to show the performance differences between them. Discussing the electrostatic capacitance based on AAO substrate, and then comparing the specific capacitance of electric double layer supercapacitor and pseudo supercapacitor based on flat surface and porous surface. Finding the function of the nano-holes in these capacitor. Summarizes the research work and results of this master thesis. Some future work to improve the performance will be suggested.
CHAPTER 2: ON CHIP SUPERCAPACITOR DESIGN

2.1 Electrostatic supercapacitor based on Micro/Nano structure

So at the beginning of this thesis, I put forward a new "multilayer electrostatic capacitor based on porous structure" is mainly composed of high aspect ratio structures with deep vertical trench. This structure is the three-dimensional micro-structure, formed on a silicon or the other cheap substrate. The purpose of multilayer design is to increase the surface area of the device and improve device capacitance. Finding the high specific area material as the substrate was the key point during this design. At the beginning, I try to use black silicon as the morphology of this substrate as show in figure 2.1.

![Figure 2-1: the SEM image of the porous silicon](image)

From the image we can see it very clear. It is a good structure for my requirement in the high aspect ratio, but it is not easy to deposit a multilayer on the surface and got the conformal layer during the processing. So maybe have the other structure can solve this problem perfectly[17].

If we want to get the higher aspect ratio than the other porous structures, we must try to find the configuration in Nano-scale. In recently years, Nano-scale materials are widely used because of its unique configuration and high ordering structures. So if the Nano-scale porous structure can get the high aspect ratio[3], it must be have significant potential in Micro and Nano technology. So many researchers dedicated to this research.

And AAO (anodic aluminum oxide) template is one of the representative research result in this aspect. It have the advantage for such application such as alignment porous structures, flexible fabrication processing and low cost. So it is an appropriate structure system as the capacitor substrate[5].
In 2009, Parag Banerjee, Israel Perez, and Laurent Henn-Lecordier used AAO template and ALD technology to make Nanotubular metal–insulator–metal capacitor arrays for energy storage[23]. Figure 2-2 shows the design of fabrication flow of anodic oxidation based electrostatic supercapacitor. Firstly, Si substrate will be anodic oxidized with high dense high-aspect-ratio manholes. Subsequently, ALD will be used to deposit very thin and conformal Al and Al2O3 layers, serving as the bottom electrode and the dielectric layer of the supercapacitor, respectively. Finally, another layer of Al will be deposited to function as the top electrode, the supercapacitor will be finished by two steps lithography and tching. These highly regular arrays have a capacitance per unit planar area of 10 uF cm-2 for 1-um-thick anodic aluminium oxide and 100 uF cm-2 for 10-um-thick anodic aluminium oxide, significantly exceeding previously reported values for metal–insulator–metal capacitors in porous templates. It should be possible to scale devices fabricated with this approach to[24] make viable energy storage systems that provide both high energy density and high power density.

Figure 2-2: Process sequence to prepare MIM capacitors. a, Al foil is anodically bonded to a glass substrate. b, AAO pore formation. c, MIM deposition via ALD processes. d, Electron-beam Al is deposited on top. e, Photolithography, masking and etching of the Al electrode, then the top electrode (TE) TiN, to define the capacitor area. f, Electrical testing using the Al foil (which is in contact with the bottom electrode TiN) as a back contact and electron-beam Al as the top contact. g, Two-inch wafer with capacitors of different areas defined on the surface. h, A blown-up image of an actual ‘dot’ capacitor tested. Each such dot capacitor is 125 um wide and contains 1-106 nanocapacitors.

Follow this structure, we try to fabricate a multilayer supercapacitor basic on these theory. Figure 2-3 illustration of a triple layer stack capacitor (MIMIMIM) comprising three layers
of TiN and three dielectric layers. (b) Illustration of a multilayer stack capacitor in 3-D silicon. Three TiN layers are contacted at the front side (C1, C2, and C3), whereas the backside of the wafer is used for substrate contacting. After the electrical connect part finished, there have four wiring terminals, and these four wiring terminals we can connect them in different way which according to your own requirement. Usually you combine capacitors in parallel because you want to increase the total capacitance while fitting the components in a certain position. And in the other way you combine capacitors in series circuit which can get the high voltage rating. And you also can use series capacitor to decrease the capacitance to get the smaller value which you did not have that special capacitor that you need,

First connect the wiring terminals as show in figure 2-4. in series capacitors are connected together in a single line. The charging current (\(i_C\)) flowing through the capacitors is the same for all capacitors as it only has one path to follow. So the current must be follow \(i_{ab}=i_1=i_2=i_3=\ldots\) etc. as we know \(Q=It\), therefore each capacitor will store the same amount of electrical charge, so \(Q\) on the whole capacitor have the same charge store[25]. And on each plates also have the same charges. So \(Q=Q_1=Q_2=Q_3\). And the voltage drop across all the capacitor and the individual capacitor also follow the Kirchoff’s Voltage Law, so from
the law (KVL) we get:

\[ V_{ab} = V_1 + V_2 + V_3 \]

\[ V_{ab} = \frac{Q_{ab}}{C_{ab}} = \frac{Q_1}{C_1} + \frac{Q_2}{C_2} + \frac{Q_3}{C_3} \]

From \( Q = CV \) we can get the series capacitors equation as follow:

\[ \frac{1}{C_{ab}} = \frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3} \]

Then, the total or equivalent capacitance of a containing capacitors in series we can calculate like that the reciprocal of the whole capacitances Figure2-5 equal the reciprocal of all of the individual capacitance’s added together.

Because of the sum voltage of the circuit equal the individual voltage added together, so the capacitors connect in series chains will increase the afford voltage in the whole circuit. So that is the advantage we can use it to share the voltage when there have a high voltage between the capacitor. So that why we choose this connect mode.

Second, we can connect the individual capacitors in parallel pattern, as shown in figure 2-6. As we know, the parallel circuit has the same the voltage drop between the circuit elements. Then we get:
\[ V_{ab} = V_1 = V_2 = V_3 \quad (2-1) \]

The current flowing go through the primary route equal to the sum of branch current. That must be followed the Kirchhoff’s Current Law (KVL). So we can get:

\[ i_1 = C_1 \frac{dv}{dt} \quad (2-2) \]
\[ i_2 = C_2 \frac{dv}{dt} \quad (2-3) \]
\[ i_3 = C_3 \frac{dv}{dt} \quad (2-4) \]
\[ i_{ab} = C_1 \frac{dv}{dt} + C_2 \frac{dv}{dt} + C_3 \frac{dv}{dt} \quad (2-5) \]

Because of the same voltage drop at the different terminal, so we can write it as follow:

\[ i_{ab} = (C_1 + C_2 + C_3) \frac{dv}{dt} \quad (2-6) \]
\[ i_{ab} = C_{ab} \frac{dv}{dt} \quad (2-7) \]
\[ C_{ab} = C_1 + C_2 + C_3 \quad (2-8) \]

So we for the parallel mode, the capacitance equal to the sum of all the capacitance. In the other words, we can see from figure 2-6, the top plates of each capacitor connect together in parallel connect mode. And the bottom plates of each capacitor also connect together. That means the effective plate area was increased because of the three plates were touching each other and equal to one single palate, as we know, capacitance is related to plate area \( C = \varepsilon A/d \), the capacitance value of the combination will also increase. Then the total capacitance value of the capacitors connected together in parallel is actually calculated by adding the plate area together. In other words, the total capacitance is equal to the sum of all the individual capacitances in parallel. You may have noticed that the total capacitance of parallel capacitors is found in the same way as the total resistance of series resistors. Those capacitor were connect in parallel with the advantage which can quietly increase the capacitance because of the effective area. This is the starting point why we design my device in this pattern.

### 2.2 Electrochemical supercapacitor design based on Micro and Nano structure.

Based on the AAO substrate, we also can fabricate the electrochemical supermirror. First we can fabricate electric double layer supercapacitor based on AAO. The electrode materials we can chose gold or copper. Then use sputtering to deposit these materials on the top surface. In spite of sputtering do not have the good conformity. We still use it instead of ALD due to the master project which we try to use the instrument in our lab. During the process of sputtering, we try to use rotation to get a conformal film on the top side. The schematic as show in figure 2-7. After electric double layer capacitor. People invented the faradaic capacitor, also called pseudo capacitor. That was on the electrode surface and bulk. During the pseudo-capacitance material loading process[11]. We do the
electrochemical CV cycle deposition and deposited MnO$_2$ on the top side of electrode structures\[10][14]. And the schematic was show in figure 2-8.

2.3 Overall scheme design

In this thesis, from the design of MEMS storage devices, manufacture the MEMS capacitor with high-performance, large-capacity volume ratio, and development of the process based on the MEMS technology and looking for a better way to get a high aspect ratio micro supercapacitor which have a high performance in energy storage, the overall design approaches as blow. Due to the basic principle of the capacitor. Greatly increase the capacitance have three basic perspective. One is increase the effective area of the electrodes. The other is increase the dielectric constant of dielectric materials, at the same time we should increase the electrical conductivity of the electrodes. Last one is decrease the distance between two electors. According to these points, we design the overall scheme process as show in figure 2-9.
Explore and processing advanced substrate with high-aspect ratio

Optimization the porous structures

Using the SEM and AFM to test the characteristic parameter

Find the suitable technology for electrode processing

Fabricate the electrostatic device based on this structure

Using electrochemical test analyze the advantage of this substrate

Grow active material on the electrode to make faraday supercapacitor

Compare the double layer capacitor based the on AAO substrate and flat substrate

Fabricate double layer supercapacitor based on the this substrate

Using C-V and I-V analyzed the property of the capacitor

Figure 2-9: Overall schematic design process of the thesis
CHAPTER 3: TECHNOLOGY FOR FABRICATION OF ON-CHIP SUPERCAPACITORS AND SETUP FOR EXPERIMENT

3.1 Sputtering techniques.

Sputtering is a technique used to deposit thin films of a material such as Au or Cu onto a substrate such as a silicon wafer. It is a physical vapor deposition method. By first creating a gaseous plasma and then accelerating the ions from this plasma into some source material which we call that target, the target is eroded by the arriving ions via energy transfer and is ejected in the form of neutral particles - either individual atoms, clusters of atoms or molecules. As these neutral particles are ejected they will travel in a straight line unless they come into contact with something - other particles or a nearby surface. If a "substrate" such as a Si wafer is placed in the path of these ejected particles it will be coated by a thin film of the source material. The principle as show in Figure 3-1.

So as show in sputtering, the target material and the substrate is placed in a vacuum chamber. Between them there have a voltage and the target is the cathode and the substrate is attached to the anode. A plasma is created by ionizing a sputtering gas which we usually use a chemically inert, heavy gas like Argon. After that the sputtering gas bombards the target and sputters off the material we’d like to deposit[26]. Depending on the way of plasma generate, sputtering can be divided into DC glow discharge sputtering, RF sputtering and plate magnetron sputtering. DC sputtering is generated by a DC electric field and then give the acceleration, the system is very simple;

![Figure 3-1: The basic principle diagram of sputtering](image)

RF sputtering is used to generate a radio frequency electric field and accelerate the gas...
plasma, and then collision followed the electronic shock way, and it is very easy to couple to the reaction chamber by any impedance. In the RF electric field, the solid surface will suffer the free bombardment under the gas ions. Magnetron sputtering is the mainstream sputtering technology. In the front of the target added a magnetic field that can control the electrons along the surface of the cathode in the spiraling magnetic field direction, there would have a significant increase in the probability of collision of ions and ionization rate, the deposition rate also increases several times. The deposition rate is also proportional to the sputtering yield, as show in the Figure3-. An optimum pressure exists for high deposition rates in the red spot area. Higher pressure means more collisions and ions but more scattering will happen. Reverse, lower pressure means less scattering but less collisions and ions. Therefore, you should try to find an optimized point to balance this relationship.

The advantages of sputtering. First, it is not a line of sight method, it can use diffusive spreading for coating and can coat around corners. Second, it can process alloys and compounds include tin alloys and silicon oxide. Even organic compounds have been sputtered. High temperatures are not needed. So during the process of deposition, you can use photoresist or the other materials to protect you structure. Then it can coat large areas more uniformly. However, there still have some limited condition such as the pressure or the target area. Angular distribution of sputtering depends on the pressure. Because the lower pressures result in a more directed flow that results in less uniform films and higher pressures result in more isotropic flow and better coverage. Uniform films also require larger targets. Large target sources mean less maintenance.
3.2 Ion milling

In order to obtain a smooth cross-section which was facilitated to observe the sectional structure when we use SEM. Because when we use scissor or the other cutting techniques to make a cross section. And there will be have a significant lateral shear forces to the sample and lead to the cross section crash. Near the cross section will have uneven phenomenon such as delamination, scratches, smearing and covered by particles, etc. all of these will impact the observation.

![Figure 3-3: The cross section of the ion milling](image)

Ion milling system is a stress free physical process, and the atoms come from the target material and bombard the target by energized particles. On the part of the sample there have an ion beam resistant mask that will avoid sample being etched. Moreover, the other place that have no mask protect will removed by the energized particles and get mirror-surface quality cross sections as show in Figure3-3.

3.3 ALD technology

Atomic layer deposition (ALD), formerly called atomic layer epitaxy, was developed in the 1970s to meet the needs of producing high quality, large-area flat that used at display with perfect structure and process controllability. It is a technique capable of depositing a variety of thin film materials from the vapor phase. Based on sequential, self-limiting reactions, ALD offers exceptional conformality on high aspect ratio structures, thickness control at the Angstrom level, and tunable film composition. In my essays, creating nanomaterials and making nanostructure with Nano porous structural perfection is an important goal for my design in nanotechnology. So for the deposition we should choose ALD technology to get a conformality layer[27].
The principle of ALD is that there have alternate saturation reaction on the substrate, an independent precursor gas entry in the reaction chamber and react with reflect precursor which absorbed on the substrate surface. In ALD technology, due to the reaction precursor flow into the reaction chamber by itself that is control by a continuous pulsed. When the reaction was saturated on the substrate surface, the flow will be stopped. And they will be had a chemistry absorption and the reaction will be occurred on the surface. Between the pre-precursor pulses there will use an inert gas to clean the reactor chamber. It is a key process we can make sure whether the pre-precursor material can have a chemically absorbed to achieve the atomic layer deposition. As show in the Figure3- , it is about the gas adsorption characteristics on the matrix material surface[28]. We can see that any gas phase material can be physically adsorbed on the surface. But if we want to get a chemical adsorption, we must have a certain activation energy. Therefore, atomic layer deposition can be achieved or not decide by the precursor which we choose. So it is a very important point in the process.

As show in the Figure3- is a reaction cycle for the atomic layer deposition. By a pulsed manner, the first reactive precursor (H2O) flow into the reaction chamber and chemisorbed on the substrate until the adsorption saturation. And the excess reactive precursors are purge out of the reaction chamber by the inert gas[29]. And then the second reactive precursor for example Zn(C2H5)2 followed the same pulsed manner flow into the reaction chamber, and react with the last adsorbed on the surface of the precursor. Waiting until the reaction is complete. After that the excess reactants and byproducts is purge out of the reaction chamber by inert gas again[30]. Because the atomic layer thin film deposition technique is an alternately saturated gas-solid phase surface reaction, so ideally, each film growth is a single atom layer, no other impurities generated, have so many advantages such as good retention, consistency, repeated and digital precise controllability, etc.

In atomic layer deposition technique, film growth pattern can be divided into three types: two-dimensional growth; island growth; random deposition. First, two dimensional growth mode((F-M Mode)): follow the mechanism of ALD, a thin film layer deposited layer by
layer on the two-dimensional growth mode, and the deposition of thin film growth is always having a priority in the lowest layer, the grown single layer covering on the whole substrate[31]. Second is the layered - island growth. Island growth mode is the film deposited on the substrate with selection property. The ALD initial nucleation is mainly followed the island-like pattern, new deposition material tend to selectively grown on the material, which deposited in last cycle growth, the process of merging the island tend to be a film thickness of up to several tens of nanometers when it can be finished. During the island structure merge into a thin film. Due to the crystal lattice mismatch, big differences of surface free energy will produce a large number of grain boundaries, and ultimately generate a polycrystalline structure. Last is the Random deposition[32]. Eeposition is random statistical mode of growth, it followed the statistical growth mechanism, they have the same probability when a new material deposited on the entire surface of the substrate position, atomic layer deposition is grown in self-limiting growth pattern, so the random deposition of the growing film looks more uniform than the other two pattern formation.

![Figure 3-5: a reaction cycle for the atomic layer deposition](image)

The atomic layer deposition have the temperature requirements. The temperature of atomic layer deposition reaction is generally in the 200-400 degree. the reaction temperature is too high or the precursor reaction product easily decomposed or desorbed from the surface. It will affect the quality of the deposition and reduce the reaction rate, the reaction temperature is too low, the precursor due to surface chemical adsorption and reaction barrier effect and difficult to sufficiently adsorption and reaction in the substrate surface, and even condensation reactive substances, thus seriously affecting the deposited layer quality. Reduce the reaction rate. Figure 0 indicates normal reaction of atomic layer deposition process can be completed within a suitable temperature range[33]. Otherwise,
the deposition rate and the film quality is difficult to guarantee.

The ALD process takes place in a so-called ALD temperature window. The reaction is generally in the 200-400 range. Figure 3-6 shows a general temperature window of an ALD process. The substrate temperature must be high enough (higher than $T_1$) to prevent condensation of any of the reactants. If condensation occurs during an ALD cycle, undesirable or uncontrollable reactions might happen, resulting in the formation of porous and impure films. Moreover, in several types of surface reactions an activation energy has to be exceeded. Therefore, a minimum substrate temperature ($T_1$) is also required to proceed with the ALD process. However, an undesirable decomposition of a reactant will happen if the temperature is too high (higher than $T_2$)[23]. Furthermore, CVD reactions will start to occur, which leads to an uncontrolled deposition of the film. Re-evaporation is another effect which becomes more likely at higher temperatures and which may result in a decreasing GPC versus temperature. Due to the above characteristics, ALD finds applications in the preparation of high-quality thin films, especially when excellent step

![Figure 3-6: a general temperature window of an ALD process.](image)

coverage and/or low processing temperatures are required.

Atomic Layer Deposition Advantages
Atomic layer deposition (ALD) has several advantages over other techniques due to the actual mechanism used to deposit thin film coatings. ALD is especially advantageous when film quality or thickness is critical[32]. ALD is also quite effective at coating ultra-high aspect ratio substrates or substrates that would be difficult to coat with other thin film techniques.

1. Atomic Layer Deposition for Perfect Films
   - Digital thickness control to the atomic level by depositing film one atomic layer at a time
   - Pinhole-free films, even over very large areas
   - Excellent repeatability
   - Wide process windows (no sensitivity to temperature or precursor dose variations)
   - Low defect density
   - Morphous or crystalline, depending on substrate and temperature
- Digital control of sandwiches, heterostructures, nanolaminates, mixed oxides, graded index layers, and doping
- Insensitivity to dust (and ability to grow underneath dust)
- Standard recipes for oxides, nitrides, metals, and semiconductors
- 100% film density guarantee for ideal material properties

2. Atomic Layer Deposition for Conformal Coating
   - Perfect 3D conformality, 100% step coverage: uniform coatings on flat, inside porous, and around particle samples
   - Atomically flat and smooth coating that copies shape of substrate perfectly
   - Large area thickness uniformity
   - Easy batch scalability (precursor sources are small and allow stacking of substrates)

3. Atomic Layer Deposition for Challenging Substrates
   - Gentle deposition process for sensitive substrates, no plasma needed (though it is available as an option)
   - Low temperature deposition possible (RT-400 °C)
   - Coats everything, even on Teflon
   - Excellent adhesion due to chemical bonds at the first layer
   - Low stress due to molecular self-assembly

3.4 Thermal evaporation

Thermal Evaporation is one of the common techniques during the Physical Vapor Deposition (PVD). Material is heated in a vacuum chamber until its surface atoms have sufficient energy to leave the surface. At this point they will travel the vacuum chamber directly to the target object, at thermal energy, and coat a substrate positioned above the evaporating material (average working distances are 200 mm to 1 meter). The material vapor finally condenses in form of thin film on the cold substrate surface and in the top of the vacuum chamber walls. Usually there must be keep in low pressures, about 10^{-6} or 10^{-5} Torr, to avoid reaction between the vapor and atmosphere. At these low pressures, the mean free path of vapor atoms is the same order as the vacuum chamber dimensions, so these particles travel to the substrate directly like in straight lines from the evaporation source. This originates 'shadowing' phenomena with 3D objects, especially in those regions not directly accessible from the evaporation source (crucible). Besides, in thermal evaporation techniques the average energy of vapor atoms reaching the substrate surface is generally low (order of kT, i.e. tenths of eV)[34]. This affects seriously the morphology of the films, often resulting in a porous and little adherent material.

The basic steps of thermal evaporation process
1. Heating and evaporation process. Including the phase transition from condensed phase to the gas phase (solid or liquid to vapor). Each materials have different saturated vapor pressure when they evaporate in different temperature.
2. The atoms and molecules transmit between the substrate and the evaporation source. During the flight, the number of the collision with the residual gas molecules in the vacuum chamber depends on the mean free path of evaporation atoms and the distance between source and substrate.
3. Evaporation atomic or molecular deposit on the substrate surface, namely steam condensation, nucleation, nucleation, and growth, form a continuous film. Since the substrate temperature is much lower than the evaporation source, the molecular deposit occurs directly from the gas phase to the solid phase transition.

4. The character of thermal evaporation
   - The device is simple, easy to operate
   - The film with high purity, good quality, thickness can be accurately controlled
   - Deposition speed, high efficiency, using a mask can get a clear graphics
   - Mechanism for the film growth is relatively simple

5. The main disadvantage of this method is that: It is not easy to obtain a crystalline structure film; adhesion is not good when film formed on the substrate, process repeatability is not good enough.
   A. Thermal evaporation deposition
      This is done inside a vacuum chamber where the material, usually in a boat is heated typically to its melting point and the substrate to be deposited on is positioned facing the source a couple feet away. A high current flowing through the boat heats it up and causes evaporation. A crystal monitor is mounted close to the substrate, which provides an estimate of how much and how fast the material is being deposited. The distance between the source and the substrate is wide to prevent solid particles reaching the substrate.
   B. electron beam evaporation
      This typical physical vapor deposition (PVD) process is also performed in a vacuum chamber. A high dc voltage is applied to a tungsten filament that causes electrons to be discharged. The stream of electrons emitted excites the targeted solid and turns it into vapor, which travels to the substrate. As they reach the surface, they condense and form a thin film coating. The advantage of EBCVD
      - High density of the electron current can be obtained the greater energy density than the resistive heating source.
      - The material is drop in the evaporation crucible which use water cooling, to avoid gasification and the reaction between container material and the evaporation materials to improve the purity of the film.
      - Heat is applied directly to the surface of the vapor deposition material, high thermal efficiency, low heat radiation and heat conduction loss

6. Compare different deposition methods as show in Table 3-1.

**Table 3-1: comparative table of different deposition methods**

<table>
<thead>
<tr>
<th>Techniques</th>
<th>ALD</th>
<th>CVD</th>
<th>Sputtering</th>
<th>Evaporation</th>
<th>PLD</th>
</tr>
</thead>
<tbody>
<tr>
<td>Uniformity</td>
<td>Good</td>
<td>Good</td>
<td>Good</td>
<td>Normal</td>
<td>Normal</td>
</tr>
<tr>
<td>Density</td>
<td>Good</td>
<td>Good</td>
<td>Good</td>
<td>Not good</td>
<td>Good</td>
</tr>
<tr>
<td>Step coverage</td>
<td>Good</td>
<td>Polytrope</td>
<td>Not good</td>
<td>Not good</td>
<td>Not good</td>
</tr>
<tr>
<td>Quality</td>
<td>Good</td>
<td>Polytrope</td>
<td>Not good</td>
<td>Not good</td>
<td>Polytrope</td>
</tr>
<tr>
<td>Low temperature</td>
<td>Good</td>
<td>Polytrope</td>
<td>Good</td>
<td>Good</td>
<td>Good</td>
</tr>
<tr>
<td>deposition</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Deposition rate</td>
<td>Not good</td>
<td>Good</td>
<td>Good</td>
<td>Good</td>
<td>Good</td>
</tr>
</tbody>
</table>
In this thesis, I should use the film deposition techniques to make a multilayer on the surface of nanostructure of AAO template. Compare the characters of different technology in the table 3-1, ALD is the best chose for conformal film on the porous structure. I will use ALD to deposit the HfO2 and TiN as dielectric layer. But in our lab have no ALD process, so if we want to make a multilayer is impossible on the porous structures. In order to simulate this multilayer structure. We fabricate a simple multilayer capacitor based on flat silicon wafer.
CHAPTER 4: FABRICATING EXPERIMENTS

4.1 The mechanism of anodic oxidization

The research about AAO films starting in the 1750s, initially the main goals research about anodizing aluminum substrate in order to improve corrosion and wear resistance performance. 50 years ago, AAO with regular-hexagonal pores was first reported. Several years later, with the continuous development of new testing technology. At the same time, the film is clearly understood along with going deep into of research gradually. So many fundamental mechanism for regular pores formation was proposed. Researchers try to analyze this formation mechanism from different disciplinary perspectives such as thermology, electrode kinetics and hydromechanics. and various of theoretical models were established. Straight has said, continued to have a new formation mechanism is established, such as Keller model, O’sulliavan model and Thompson model , Parkhutik model and electric field mode etc. Until now, still have new formation mechanism was established. But in academic world, there are no final conclusion has yet been reached on the film formation, the following is just my own thinking which conclude from so many theoretical models[35][36].

4.1.1 The theory of the porous layer formation

High electric field ion conductor is the driven force for the film growth. The electric field intensity is very high when the anodic oxidization, almost reach to $10^7$ V/cm. High electric field products ion current. Oxidation film continuous growth on the interface because of the partials movement. There is the relationship between ion current and electric field.

\[ i = A e^{B E} \]  

(4-1)

In generally believed that aluminum in acid or weak alkaline solution can form porous membrane. The reaction mechanism in acid solution as follow.

Anode:

\[ \text{Al} \rightarrow \text{Al}^{3+} + 3e \]  

(4-2)

\[ 2\text{Al} + 30^{2-} \rightarrow \text{Al}^{3+} + 6e \]  

(4-3)

Cathode:

\[ \text{H}^+ + 2e \rightarrow H_2 \]  

(4-4)

At the beginning of the membrane growth, Al$^{3+}$ dissolve into the solution. At the interface of theseolution and film have the reaction like this. In my experiment I used phosphoric acid. Under the effect of the electric field. Al$^{3+}$ out-migration. O$^{2-}$/OH$^-$ in-migration. Al$^{3+}$ directly dissolve into solution after through the oxidization film. there will formed oxide film after OH$^-$/O$^{2-}$ entering the oxidization film and react with aluminum at the interface.

\[ \text{Al}^{3+} + \text{PO}_4^{3-} \rightarrow \text{AlPO}_4 \]  

(4-5)

During the process of AAO membrane formation. Alumina is constantly being dissolved on the interface between electrolyte and oxide layer. Aluminum is constantly oxidized on the interface between aluminum and oxidization film.
The chemical reaction equations as follow:

\[ \text{Al}_2\text{O}_3 + H_2O \rightarrow Al^{3+} + O^{2-} + OH^- + H^+ \] (4-6)

There will formed double-barrier-layer structure during this chemical reaction processing. Interior layer contained anion and external layer without anion. Under the condition of the stably anode voltage, there have a balance between formation rate and dissolution rate about the barrier layer. The barrier layer would reach to stable thickness by self-adjustment. The electric field was enhanced between electrolyte and oxidization layer when the applied voltage increasing. The hydrolysis rate will speed up[37]. And it will lead to accelerate the growth of oxide layer. And this will thicken the barrier layer and led to the voltage increase which effect on this part. So the electric field between electrolyte and oxide layer will descend. Consequently the stable growth state under the thicker barrier layer come into being. On the contrary, when the applied voltage reduced. The opposite state which described previously will occur. Barrier layer growth keep a stationary value under the steady anode voltage. Eventually regular tubes array morphology structure will be formed. Show as in Figure 4-1, the chemical reaction processing of the anodic oxidation formation during this processing, with the development of anodic oxidization. The oxide film on the aluminum surface became thicken. Because of the stress concentration on the alumina surface, there will be formed defect. So the current density was bigger than the other place. The reaction will happen in this place first. Porous structure form following alumina dissolution[15].
4.2 Fabrication of AAO template

All the design basic on the AAO template, so each the AAO template is the first step I should finish, preparation steps as follow.

4.2.1 Preparation of electrolyte and electrochemical process

**Aluminum substrates:**
High quality aluminum substrate is an important impact factor in the process how to get a high ordered porous aluminum dioxide template. Cubical dilatation model regard as the orderly nanopore of alumina membrane due to the mechanical stress of the volume expansion in the process. Thus, when we choose foil should follow these conditions as follow: (1) the aluminum has single structure and composition. Have no inner mechanical stress, low surface roughness. So as to eliminate the local volume expansion and uneven distribution of stress in the processing as much as possible. In order to generate the oxide film with bigger area[38]. I choose polycrystal aluminum and the size such as: 1 cm width, 2 cm length and 0.15 thickness. And the purity more than 99.999%, (bought it from sigma)[39].

**Electrolyte:**
High quality electrolyte also is very important impact factor during the processing for the regular structures[40][41]. The impurity factor in the electrolyte will influence the anodic aluminum membrane growth in different degrees[42]. Especially the chloride ion will make oxide film loose. Produce local corrosion. Even more cannot form oxide film. We use DI water as the solvent, and use analytic reagent such as phosphoric acid, oxalic acid as electrolyte. And the concentrate is 0.2mol.L⁻¹ and 0.4 mol.L⁻¹ respectively[43][44].

<table>
<thead>
<tr>
<th>Table 4-1: The materials for AAO fabrication</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>aluminum substrates</strong></td>
</tr>
<tr>
<td>Polycrystalline aluminum foil</td>
</tr>
<tr>
<td>Thickness 0.1mm and 0.15mm, Width 150mm, Purity&gt;99.99%</td>
</tr>
<tr>
<td><strong>Electrolyte</strong></td>
</tr>
<tr>
<td>Deionized water resistivity less than 15MΩ.cm as solvent</td>
</tr>
<tr>
<td>analytical reagent (phosphoric acid, vitriol, oxalic acid) as electrolyte, and the concentrate as 0.2mol.L⁻¹, 0.3mol.L⁻¹, 0.4mol.L⁻¹</td>
</tr>
</tbody>
</table>

All the chemical solution and instrument I will use in my experiment, Constant temperature system: Water bath heating system, power systems: Continuous adjustable dc regulated power supply, cathode material: Pt (platinum99.99%). Other chemical reagent used for cleaning, polishing, etching, moving prevent layer. All the chemical reagent use AR.

<table>
<thead>
<tr>
<th>Table 4-2: The chemical reagent for AAO fabrication</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Name</strong></td>
</tr>
<tr>
<td>molecular formula</td>
</tr>
<tr>
<td>Chemical</td>
</tr>
<tr>
<td>-----------</td>
</tr>
<tr>
<td>Acetone</td>
</tr>
<tr>
<td>Ethanol</td>
</tr>
<tr>
<td>Perchloric acid</td>
</tr>
<tr>
<td>Oxalic acid</td>
</tr>
<tr>
<td>Sulfuric acid</td>
</tr>
<tr>
<td>phosphoric acid</td>
</tr>
<tr>
<td>chromic acid</td>
</tr>
<tr>
<td>Copper(II) chloride</td>
</tr>
</tbody>
</table>

**Power source:** we used VWR power supply. Supply voltage can adjust continuous in the range which form 0 volt to 250 volt. And in the cathode we connect it to a platinum electrode. In Figure 4-5 is the voltage source.
**Tube Furnace High Temperature 2 inch:** The furnace (as shown in Figure 4-5) temperature varies from room temperature to 1000°C. Gases that can be connected are O2, N2 and H2 and forming gas. Normally only one gas at the time. Annealing in vacuum is also possible (optional).

**SEM Hitachi:** The SU3500 Scanning Electron Microscope features innovative electron optics and signal detection systems to provide unparalleled imaging and analytical performance. All new electron optics design with best-in-class image sharpness. 7 nm SE Image Resolution at 3 kV, 10 nm BSE Image resolution at 5 kV. As shown in Figure 4-5.

**Ion Milling Im4000:** The Hitachi IM4000 Ar ion milling system as shown in Figure 4-5, and Sputter AJA. AFM XE-200, Electrolysis equipment constructed by myself: As shown in figure 4.6 include magnet stirrer and platinum electrode.

### 4.2.2 Two-step anodization processing

The preparation technology of AAO porous substrate includes three main processes: preprocessing\[45\][46][47], anodic oxidation processing and post-processing. We can see from the flow chart as follow in Figure 4-6:

(Figure 4-6: Two-step anodization processing)

(1) Preprocessing of the aluminum foil
a. We use acetone to remove the surface grease after cutting aluminum foil. Then we use ethanol in an ultrasonic cleaning machine to clean. After that using nitrogen dry it. During this process, we should take care about the surface of foil. Do not destroy the surface. Otherwise, the current flow will focus on the defective parts during anodic oxidation process lead to sample the ablation.
b. Put the samples into 2-inch furnace chamber, and then we choose nitrogen environment. Heating rate we chose 10 degrees/second. In addition, kept in 480 degree for 5 hours. The purpose of annealing is to reduce the mechanical stress inside the aluminum foil. It is also can make the surface of aluminum more smooth, have less lumps. This process will increase the crystallite dimension. Fundamental purpose is formed well-aligned hexagonal structure. Furnace coupled with natural cooling with the aluminum foil inside. Took the samples out when the chamber reached to room temperature. From the experiment result, we will see there have a significant influence on the improvement of smoothness. The crystal size and flatness in proportion to the annulling time and temperature. And crystal boundaries became less and less clear accompany with the annulling time and temperature.

c. Polishing with electrochemical solution. After annulling processing still have projecting part on the surface. In order to further optimize the surface and dissolve the raised in microcosmic surface. We choose this method which with a simple equipment trait. It can polishing arbitrary object with complex structure because of this liquid polishing. The key core to this strategy is how to control the polishing time and concentration of the polishing solution. In this project, I will use Perchloric
acid and Ethanol with 1:4 volume ration. And aluminum as the anode, platinum as cathode, external voltage we used 20 volt supplied by the equipment of VWR power source. But in this process you should pay more attention on the polishing time. You can see this reaction happened very quickly. If you time is too long, there will have corrosion pit on the surface because for the over-polishing. This phenomenon would lead to pitting corrosion since the concentration of electrode current. Otherwise, if you keep in a short polishing time. You cannot attain your goal. You cannot corrode the crystal boundaries out. After polishing, turn off the switch first, and then rinse the impurity on the surface of sample by water and deionized water. And then immersed in deionized water for several minutes. Figure 4-7 which is the SEM image about the roughness of surface. You can see clearly, before polishing, compare the SEM image before and after polishing. There have a significant change on the surface of the sample.

**Figure 4-9:** I-t curves under the different oxidization voltage during the oxidation process

**Figure 4-10:** after removing the first oxidization layer

4-7 which is the SEM image about the roughness of surface. You can see clearly, before polishing, compare the SEM image before and after polishing. There have a significant change on the surface of the sample.
d. Anodic oxidation process. There have two times oxidation process. Both of them

Figure 4-12: The surface morphology of AAO image under SEM

A  B  C  D
use the same instrument as show in Figure 4- 8 (a) and (b), figure (a) is the simplified circuit, and figure b is the physical map.

We take the sample from deionized water which we prepared before, and dried it use nitrogen flow. Then used this sample as anodic of the electrodes. Used platinum as the cathode of the electrodes. The surface the aluminum directly facing the surface of platinum. And keep a distance of 2 cm between this two electrodes. Used oxalic acid as the electrolyte and the concentration was 0.4 mol/L. Then put the

![Figure 4-13: the surface morphology of AFM image](image)

beaker on the magnetic stirrer which can keep the temperature and concentration of the electrolyte at a constant state. Before turning on the switch of the VWR power source, you should set it into constant voltage model. And you can set the necessary voltage according to your need. Then recorded the current value every 5 seconds. Figure 4- 9 is I-t cures under the different oxidization voltage. As curve of A, B, C is the normal oxidization curve. And if the tendency follow the curve like D. That
means in the surface of aluminum sample, there have some defects which will corrode the sample because of current concentration.

e. Remove the first oxidization layer. After the first anodic oxidation process. There will generate orderly porous structure which was Alumina on the surface. And the SEM image you can see from Figure 4-10. However, you can see this structure looks small and not very regular. Then we should use chemical solution to remove this layer. Using 6w% phosphoric acid mixed with 8w% chromic acid as solution and immersed the sample for two hours. And we keep the temperature in the ice-water bath below 8°C as show in Figure 4-12. Then take it out using acetone rinsed the residual solution. And immersed the sample in water for several minutes. After removing the first oxidization layer, there will leave some regular pits on the surface from SEM image as show in Figure 4-12. And these pits served as guiding layer for the second anodizing treatment.

f. Second anodizing treatment. After removing the first oxidization layer, regular pits would appear on the surface. We call this as pre-texture for the second oxidization layer. And then do the second oxidation under the same conditions and solution as first time. And then pick up your sample and put it into ultrasonic cleaner soak with ethanol for 3 minutes. Dried it used nitrogen flow. In figure 4.10 is the surface morphology of AAO sample in different oxidation condition. Image A, B and C is the top view, and image D was observed from a inclined angle to see the cross section. There have a lot of nano tubes we can see from this side. In order to see the morphology more intuitive observation. We also use AFM to detect the surface as show in Figure 4-13.

So via the two step anodization processing, there will get the alignment of porous arrays. But during this process if we want to get the better structure. There must be optimized the steps, first step to get a pre-textured surface. And then this pre-textured specimen is used for further anodized for a high regular porous arrays.

4.3 Characterization of AAO template

4.3.1 Microstructure analysis of AAO template

A. Surface morphology analyze. As show in Figure 4-14, we can see the surface morphology very clear form top side. It can clearly display the highly ordered Nano holes. There have uniform aperture and all of have the same feature which have hexagonal structure. And we can also see that different area have the different alignment orientation about the hexagonal nano-holes. If you keep under observation. There have an obvious demarcation line between them. At the same area there have the same alignment orientation as show in the red circle. The area size depends on the size of the lattice. And the lattice size affect by the annulling time and temperature.

B. I-t cure analyze. Under the circumstances which we keep the other conditions have no
change and just have a linear variation about the voltage between the two electrodes. As show in Figure 4-15. Recoding the data of electrical current change when we set different electrolytic voltage such as 40v, 45v, 50v, respectively, at the same electrolyte concentration. All the curves presented a peak value at the beginning. After that, the current began to flatten. Eventually reached steady state current value was about 0.003A, 0.003A, 0.004A. By contrast, the current reaching stability state need less time when we supplied voltage at 50 volt. From the second half of your cycle. The reaction get into a relatively stable process. If there have drastic fluctuations about the current, which means some parts of the sample have the inhomogeneous reaction maybe will destroy the surface structure.

4.3.2 Polishing effect on oritation of porous

The aiming of polishing process was got smooth surface before we do the oxidation process.
That means after polishing we will move part of the aluminum foil where the bulges it have. And after this step, we do the oxidation process and the smooth surface was helpful for the current distribution. So if we can get the perfect flat surface, we will get the regular porous structure after oxidation. But for the polishing time it very difficult to control. Appropriate polishing time will got the smooth surface as in Figure 4-7 (b). But if the time is Time is too short or too long, we cannot got the regular structures we want. Figure 4-16 (A) was the SEM image which was after a short time polishing. There still have some bulges on the surface. And Figure 4-16 (B) was the SEM image which was after a long time polishing. You can see there have a lot of notch on the surface because of the long time corrosion. If there was the short time polishing sample, it was still can use, but when we used the long time polishing sample. During the oxidation process will destroy it. Because when we supply the current through the sample. There will have a current constriction due to the uneven surface. And after oxidation process there will have corrosion holes on the surface as show in Figure 4-17. How to control the polishing time was the crux of this.
matter. The polishing time determine by the concentration of the solution and potential between the two electrodes. So you should try to find the parameter by yourself. In this experiment, we choose 1 minute as the appropriate polishing time.

4.3.3 The influence factors of the aperture size

In order to get the sample which we need for fabricate capacitor. We hope that we can get the optimum parameters of the substrate. So we should exactly know which parameter would impact the diameter and the depth of the porous structure. First, we talk about the voltage between two electrodes. Setting a certain step for the oxidation voltage from 40v to 55v, and keeping the other condition have no change. Then we use SEM to get the SEM images as show in Figure 4-18. There also have the relation between the voltage and aperture size in Table 4-3. Used origin for data integration as show in Figure 4-19. In certain range, the radius in approximate linearly with the increase of bias voltage. Linear

![Sample 1 SEM image](image1)

![Sample 2 SEM image](image2)

![Sample 3 SEM image](image3)

![Sample 4 SEM image](image4)

Figure 4-18: SEM image about the pore radius of the samples. Sample 1: First oxidation voltage: 40V. Second oxidation voltage: 40V. Sample 2 First oxidation voltage: 45V. Second oxidation voltage: 45V. Sample 3: First oxidation voltage: 50V. Second oxidation voltage: 50V. Sample 4: First oxidation voltage: 55V. Second oxidation voltage: 55V.
scale approximately equal to 1.92nm/voltage (in a certain range). The fitting formula as show in equation (4-7)

\[ Y = 1.92x - 301 \] (4-7)

This relationship had the vital signification for preparing highly orderly substrate with specific diameter. So as to make a specified depth in a certain range is possible.

![Figure 4-19: the relationship between bias voltage and radius of the pore.](image)

**Table 4-3: the relationship between bias voltage and pore radius**

<table>
<thead>
<tr>
<th>Bias voltage/Volt</th>
<th>40</th>
<th>45</th>
<th>50</th>
<th>55</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pore radius/nm</td>
<td>46</td>
<td>56</td>
<td>65</td>
<td>74</td>
</tr>
</tbody>
</table>

**4.3.4 The influence factors of the thickness**

The thickness of the AAO substrate decided the depth of the porous structure. The whole area of the AAO substrate were consisted of nano-tubes. Figure 4-20 was the image we see from one crack of the AAO substrate. It was very clearly reveal the distribution of nano-tubes. For the requirement of the making capacitor, there must be have high aspect ratio. It means for the depth and aperture size, the deeper and larger, the better, in a certain range. The high aspect area have enough area to save charges. So AAO substrate have enough pore density to meet the demands if it also have enough pore size and depth.

In order to research the factors which can influence the depth of the holes. We also keep the other conditions unchanged and only change one variable. First, set the electrolysis voltage at constant value. There we choose 45v. This value we got from the relationship between pore size and voltage. And then we choose different electrolysis time during the second oxidation time. The value of electrolysis time is 1 hour, 2 hours, 3 hours, and 4
hours, respectively. For the first oxidation time, we set 1 hour for all of them. After

oxidizing process, making a crack in the edge of the sample and then using ion milling to acquire a flat surface in order to get a smooth morphology trait when detected by SEM. Followed by depositing gold on the cross section. As show in Figure 4-22, we can see the

Figure 4-20: the cross section of SEM image about the nano-tubes
Figure 4-22: SEM image about the cross section of the samples. All the samples have the same etching voltage. First etching voltage: 45V. Second etching voltage: 45V. The etching time. Sample 1: Reaction time: 1 hour. Sample 2: Reaction time: 2 hour. Sample 3: Reaction time: 3 hour. Sample 4: Reaction time: 4 hour.

Figure 4-21: the relationship between reaction time and thickness of the sample. depth of the pores from cross section view. In the image, you also can see the measurement
Table 4- 4: the relationship between etching time and thickness of the sample

<table>
<thead>
<tr>
<th>Reaction time/hour</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thickness/um</td>
<td>20</td>
<td>47</td>
<td>65</td>
<td>85</td>
</tr>
</tbody>
</table>

Table 4- 5: the relationship between bias voltage and thickness of the sample.

<table>
<thead>
<tr>
<th>Bias voltage/V</th>
<th>40</th>
<th>45</th>
<th>50</th>
<th>55</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thickness/um</td>
<td>23</td>
<td>29</td>
<td>39</td>
<td>43</td>
</tr>
</tbody>
</table>

Figure 4.23 SEM image about the cross section of the samples. Sample 1. First oxidation voltage: 40V. Second oxidation voltage: 40V; Sample 2. First oxidation voltage: 45V. Second oxidation voltage: 45V; Sample 3. First oxidation voltage: 50V. Second oxidation voltage: 50V; Sample 4. First oxidation voltage: 55V. Second oxidation voltage: 55V;

which we got by the stock software in SEM. Table 4- show the relationship between reaction time and thickness of the sample. Using origin for data integration as show in Figure 4- 21. In certain range, the thickness was approximate linearly with the increase of
reaction time. Linear scale approximately equal to 21.3um/hour (in a certain range). The fitting formula as show in equation (1):

\[ Y = 21.3x + 1 \quad (4-8) \]

This relationship had the vital signification for preparing highly orderly substrate. So as to make a specified depth in a certain range is possible.

Second. Just now we focus on the factor of reaction time. For the reaction voltage maybe also have the effect on the thickness. So we set the electrolysis reaction time at constant value. For the first and second oxidation, we both chose the same reaction time exactly 1 hour. And then we choose different electrolysis voltage during oxidation. But we chose the same reaction voltage for the same sample. The value of electrolysis voltage is 40v, 45v, 50v and 55v, respectively. After oxidizing process, made a crack in the edge of the sample and then used ion milling to acquire a flat surface in order to get a smooth morphology feature when detected by SEM. Followed this step we deposit gold on the cross section. As show in figure 4.23, we can see the depth of the pores from cross section view. In the image you also can see the measurement which we got by the stock software in SEM. Table 4- show the relationship between bias voltage and thickness of the sample. Used ORIGIN for data integration as show in figure 4.24. In certain range, the thickness was approximate linearly with the increase of bias voltage. Linear scale approximately equal to 1.38um/v (in a certain range). The fitting formula as show in equation (4-9).

\[ y = 1.38x - 32.3 \quad (4-9) \]

We can compare formula (2) and (3). The influence of oxidation layer by bias voltage was more obvious than reaction time. These were very useful for making controlled pore depth substrate when we combined the formula (2) and (3) together.

Figure 4.24 the relationship between reaction time and thickness of the
Third, during the measurement, we want to find the thickness of the Alumina, but how we can confirm the material in the margin is alumina. Is there have an obvious demarcation line between the alumina and aluminum. From Figure 4-22 you can see there have an obvious demarcation line between them. In order to make sure the top side was the alumina. We use EDX to do the component analysis as show in figure 4.25. It very easy to distinguish the component content of this cross section. And the component analysis results was show in table 4-6. The samples we have used in these experiments was shown in figure 4-26.

### 4.4 Summary of the growth characteristics for AAO template

In this chapter, we focused on the controlled membrane growth. Analyzed the key factors affecting the membrane growth. Providing the theoretical basis for preparation AAO

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**Figure 4-23: the cross section image under EDX mapping mode of AAO substrate.**

**Table 4-6: the EDX analysis result about the oxidation part**

<table>
<thead>
<tr>
<th>Element</th>
<th>AN series</th>
<th>Mass wt.%</th>
<th>norm. wt.%</th>
<th>Atom. at.%</th>
</tr>
</thead>
<tbody>
<tr>
<td>Aluminium</td>
<td>13</td>
<td>28.22951</td>
<td>57.85611</td>
<td>44.87475</td>
</tr>
<tr>
<td>Oxygen</td>
<td>8</td>
<td>20.56311</td>
<td>42.14389</td>
<td>55.12525</td>
</tr>
</tbody>
</table>
substrate in next step. All of this work based on the second anodic oxidation process and the other related theoretical basis. Optimizing the parameters of all the process for further using, and designing and constructing the electrolytic device for the electrolytic experiment. Also laid a foundation for the future experiment. Using SEM and AFM to observe the morphology feature of the samples. According to the analyzed result get the best result for madding capacitor in next steps.

### 4.5 Multilayer capacitor fabrication

In this thesis, I should use the film deposition techniques to make a multilayer on the surface of nanostructure of AAO template[48]. Compare the characters of different technology in the table 3-1, ALD is the best chose for conformal film on the porous structure[20]. I will use ALD to deposit the HfO2 and TiN as dielectric layer. But in our lab have no ALD process, so if we want to make a multilayer is impossible on the porous structures. In order to simulate this multilayer structure. We fabricate a simple multilayer capacitor based on flat oxidation silicon wafer[26][45].

#### 4.5.1 The process flow for fabrication of multilayer capacitor.

A. Sputtering technology was used during the multilayer capacitor fabrication[32].
   1. During this design, we will use sputtering instead of ALD[49][24] to fabricate the
multilayer capacitors. This design just simulate the structure which we do the ALD process on Mirco and Nano holes. So in this process I will make a bigger structure,

2. The overall structure as show in figure 4-27. That the final structure which we want. Under each square there has four-electrode layer and three dielectric layer, each square also have four electrical connection parts around it.

3. Figure 4-27 was the process flow when we see from the top view and cross section. During these steps, two masks will be used; one is used for the electrode layer as show in figure 4-29 A, and the other for the dielectric layer as show in figure 4-29 B.

4. After the step 2, 4, 6, rotating the mask for 90 degree and then do the deposition

Figure 4-25: the top view of multilayer capacitor fabrication flow
and the mask just use shadow mask which can make by laser cutting machine.
for the electrode layer.

5. Figure 4-28 was the sputtering flow when we used sputtering technology to deposit the metal layers and dielectric layers.

6. After fabrication there have four probes used to connect the electrodes for the electrical test.

![Figure 4-26: the schematic of sputtering process](image)

![Figure 4-27: Mask A was used for deposition metal layer
Mask B was used for deposition dielectric layer](image)
The whole process when we used ALD technology[30][40].

Between sputtering and ALD technology, there have big difference between them. When we deposit the thin film, which was electrode layer and dielectric layer for multilayer capacitors[5][50][33]. It is impossible to use shadow mask to fabricate the structures which we want during the ALD process. Because ALD process was the chemical vapor deposition process[51]. So we should use photoresist to protect the structures during the process. There also have the basic flow for fabrication electrode layer during ALD process.

1. Making four electrical connection parts. Chose one oxidation silicon wafer.
2. Spinning photoresist on the top side.
3. Exposure and developing
4. Then the ALD process will be used for TiN layer deposition.
5. Photoresist removal and you will get four electric connection part as show in the right part of figure 4-30 (5).
6. Spinning photoresist on the top side.
7. Exposure and developing

![Figure 4-28: ALD process for fabrication electrode layer](image)
8. Then the ALD process will be used for TiN layer deposition.
9. Photoresist removal and you will get four electric connection part as show in the right part of figure 4-30(9).

There also have the basic flow for fabrication electrode layer during ALD process.
1. Spinning photoresist on the first electrode layer.

<table>
<thead>
<tr>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image1.png" alt="Image 1" /></td>
<td><img src="image2.png" alt="Image 2" /></td>
<td><img src="image3.png" alt="Image 3" /></td>
<td><img src="image4.png" alt="Image 4" /></td>
<td><img src="image5.png" alt="Image 5" /></td>
</tr>
</tbody>
</table>

**Figure 4-31: ALD process for fabrication dielectric layer**

2. Exposure and developing
3. Then the ALD process will be used for HfO₂ layer deposition.
4. Photoresist removal and you will get the dielectric layer part as show in the right part of figure 4-31 (4).
5. And then for the second, third, and fourth layer, it almost the same process, just repeating the steps in figure 4-30, and figure 4-31. The final structure will be got as show in figure 4-31 (5). In the future research, if we have chance, we will do this process flow by ALD technology.

### 4.5.2 Results and discussion

Following the process which we have mentioned in the last section. The multilayer capacitor was fabricated by the sputtering machine as show in figure 4-31 (A). It based on silicon wafer. In order to have good insulation with the silicon substrate. In the first step,
we have deposited 30 nm SiO$_2$ on the surface as the insulating layer. Moreover, for the metal and dielectric layer, we deposit 20nm and 30nm, respectively. After this when we use electrochemical station check the structural integrity. There have short-circuit current between the two metal layers which used as electrode layer. That means short circuit has been happened between them. After analysis, the first reason was that the structures was too small, it not easy to make alignment by eyes during the process. In addition, the second one was that when we use shadow mask, there must be have gap between the silicon wafer and the mask. And during the sputtering, the atoms was very easy to go inside. So that will break the insulation layer. In order to solve these problems, the bigger design was used in the second sample which have the same parameters of thickness as show in figure 4-32 (B). But after testing, it still have the same question, there have short-circuit current between the two electrodes. Maybe the current was affected by the substrate of silicon wafer. There have leakage current through the substrate. So the oxidation wafer was used in the sample C which have the same parameters. But we also cannot solve the short-circuit current during the test. And after checking some reference paper. If we want to get the continuous film by sputtering, the thickness at least more than 15nm or 20nm. If the thickness is lower than this, it still have the island structure. Therefore, the film was not the continuous film. So we increased the thickness of the SiO$_2$ layer to 50nm. And the metal layer was 30nm as show in figure 4-32 (D), still have this problem. Maybe the thickness still too thin to make a continuous film. So we increased the SiO$_2$ and Au film to 200nm. Still cannot solve the problem. Therefore, we used Profilometer check the thickness of the SiO$_2$ and gold layer as show in figure 4-33. From image A and B, you can see the parameter was correct, which was almost the same with parameter we get from the sensor of the sputtering machine. The film looks uniform from the profilometer image. However, from figure C and D, you can see the thickness of SiO$_2$ have a big difference with the result we got from sputtering sensor. And the film of SiO$_2$ was very thin and roughness. It is not a continuous film, so that is the
reason why there have short-circuit current. In the other words, we can get the continuous film when we use this sputtering machine to deposit metal layer. But for the metal oxide, it very difficult to get the continuous and uniform layer.

4.6 The fabrication of AAO electrostatic capacitor

The electrodes layer preparation step:
(1) All samples should soak in acetone at least 1 hour for remove all the organic matter on the surface or in the porous structures.
(2) Put the samples in ultrasonic cleaner for 5 minutes with acetone
(3) Rinse the sample use deionized water.

Figure 4-30: the thickness of Au and SiO₂ after deposition
(4) Put the samples in ultrasonic cleaner for 5 minutes with water to make sure all the pores were open.
(5) Then dried them used nitrogen flow.
(6) Then use high temperature adhesive tape to protect the sample which place you did not want to sputtering metal on the surface. But before this you should use non-dusting whipping paper as the buffer layer to prevent the surface did not pollute by residues when you remove the adhesive tape as show in figure 4-34A.
(7) Fixed the samples on the sputtering AJA substrate and put into the chamber of sputtering.
(8) Deposited 100nm gold on the surface of samples as electrodes at room temperature. During deposition process. Table 4 and figure 5.2 was the parameter we set in this process.
(9) After sputtering remove all the protector as show in figure 4-34 B.

Figure 4-34: This is the samples after sputtering gold on the surface
A was the samples before remove the protect tape
B was the samples after remove the protect tape
(10) For electrical connection part, used silver conductive epoxy.

### 4.7 The fabrication of AAO double layer supercapacitors

The electrodes layer preparation step:
(1) All samples should soak in acetone at least 1 hour for remove all the organic matter on the surface or in the porous structures.
(2) Put the samples in ultrasonic cleaner for 5 minutes with acetone.
(3) Rinse the sample use deionized water.
(4) Put the samples in ultrasonic cleaner for 5 minutes with water to make sure all the pores were open.
(5) Then dried them used nitrogen flow.
(6) Fix the sample in the chamber of sputtering. The vacuum degree is lower than 0.06Torr in nitrogen environment. And then deposit 35 nanometer gold in room temperature. And the samples show as figure 4-35.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Pressure/Torr</th>
<th>Gas flow/scm</th>
<th>Ramp/s</th>
<th>Rate/(A/s)</th>
<th>Thickness/nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Value</td>
<td>2.14E-3</td>
<td>12</td>
<td>15</td>
<td>1.2</td>
<td>100</td>
</tr>
</tbody>
</table>

Figure 4-35 AAO samples with gold electrodes after remove the protector

### 4.8 The fabrication of flat double layer supercapacitors

The flat electrodes layer preparation step:
(1) Used hard plastic plate with flat surface as the substrate which had the well insulating properties.
(2) Used electrical cutter to make a smaller sample which have the same dimension compared with the AAO sample.
(3) All samples should soak in acetone at least 1 hour for remove all the organic matter on
the surface or in the porous structures.

(4) Put the samples in ultrasonic cleaner for 5 minutes with acetone.
(5) Rinse the sample use deionized water.
(6) Put the samples in ultrasonic cleaner for 5 minutes with water to make sure there have a high purity surface when we do the sputtering process.
(7) Then dried them used nitrogen flow.
(8) Fix the sample in the chamber of sputtering. The vacuum degree is lower than 0.06Torr in nitrogen environment. And then deposit 35 nanometer gold in room temperature. All the parameters were same as the AAO double layer electrode process.

4.9 Growth of MnO$_2$ on the AAO template coated with gold surface

Manganese dioxide has been widely used in the battery industry because of its low cost, wide raw material sources, good electrochemical performance, environmentally friendly[19]. As the active electrode materials of electrochemical capacitor also has a great application prospect. There have a lot of methods for making manganese dioxide[25][7]. Such as chemical methods[14], Potassium permanganate reduction method and electrolyte. The anode electrochemical deposition is a new methods for preparing manganese dioxide in recent years. We use gold layer as anode. And did anode electrolysis in manganese acetate solution[3][12].

A. C-V cycle electrolytic preparation of MnO$_2$ electrode based on the substrate with gold layer

1. Used AAO substrate or flat substrate with gold layer after sputtering which we prepared before as anode. And used deionized water to clean, then dried it in room temperature. There was also need waterproof glue to protect the area have no

![Figure 4-36: C-V cycle method loading MnO$_2$ on the electrode](image)
2. Prepared 200ml manganese acetate solution and the concentration of this solution was 0.05mol/L.
3. Also prepared 200ml sodium sulfate and the concentration of this solution was 0.1mol/L.
4. Mixed these two solution together with a certain ratio.
5. Use AAO substrate with gold layer as working electrode, silver chloride electrode as the reference electrode, platinum as the auxiliary electrode. Used Zahner IM6 Electrochemical workstation as the power source and the experimental set-up as show in figure 4-36. We choose three electrode test mode. The beginning and ending voltage we choose 0.4 volt. And the scanning interval of voltage we chose 0.3 volt to 1.3 volt. And the sweep rate we chose 100mv/s for 20 cycles.
6. Figure 4-37 is the sample after deposited MnO2 on the surface.

Figure 4-37: sample A and B is the sample after deposited MnO2 on the surface. Sample C is the flat substrate with gold layer.
5.1 test the performance of the electrostatic capacitor and electrode

5.1.1 The principle of cyclic voltammetry

Cyclic voltammetry is one of the commonly method we usually used to test the electrode of capacitor[23][11]. Double layer of the supercapacitor can be equaled to the parallel plate capacitor[6]. According to the formula of the parallel plate capacitor as show in figure 5-1.

\[ C = \frac{\varepsilon S}{d} \]  
(5-1)

- $C$----capacitance. Unit: F
- $\varepsilon$-----dielectric constant.
- $S$------opposite area between two electrodes. Unit: m².
- $d$-------the distance between two electrodes. Unit: m.

Thus, double layer capacitor affected by the availably area and the thickness of the double layer. And the availably area related with the aspect ratio of your porous substrate. So after the fabricate process of your electrodes. The capacitance will be determined. As we know as follows:

\[ i = \frac{dQ}{dt} \]  
(5-2)

\[ C = \frac{q}{U} \]  
(5-3)

From these two formulas we got:

\[ i = \frac{dQ}{dt} = C \frac{dU}{dt} \]  
(5-4)

- $i$------current. Unit: A
- $dQ$----Charge differential. Unit: C
- $dt$-----time differential.
- $dU$----potential differential

so, if we provide electric potential on the electrode. There will have a responded signal of current. Cyclic voltammetry is the test method which supplied a linear variation potential signal when doing the test. And check the signal about the current change. And we can get information from the diagram with these two variations.

In that case, the sweep rate was a constant. There would have a directly proportional relationship between current I and the capacity of the electrode. That is to say, for a given electrode. Under a certain sweep rate test the electrode using cyclic voltammetry. Through the current change from vertical coordinates. We can calculate the capacitance of the capacitor. And got the specific capacitance.
5.1.2 C-V testing on AAO electrostatic capacitors

The main performance of capacitor is to store charge. Under the power supplied by the outer circuit. On the two electrodes gathered the same amount charge which have opposite charge. When we withdraw the power source. The charge would store in the electrode. Except the property of capacitance. The capacitor also have the inductance and resistance properties. Under the low frequency signal, Inductance and resistance characteristics influence on the device can be ignored. But under the high frequency signal, Resistance and inductance characteristics will lead to capacitance dissipation. Aimed to test the characteristics of the capacitor. In my article I mainly used cyclic voltammetry to test the C-V curve and I-V curve and the cycle-to-cycle stability.

We used Zahner IM6 Electrochemical workstation to test all the parameters. And we chose two electrode mode to test the electrostatic capacitor as show in figure 5-1. There three types of electrostatic supercapacitor we would test. The first one is the top side of AAO substrate with gold layer. The gold layer based on AAO porous structure is one of the electrode in this device, and the other one is the aluminum which had not reacted with the electrochemical solution. These two metal layer were the electrode of the capacitor. For the second one. We know during the AAO fabrication. We use electrochemical etching to make the hexagonal structures, in the back side of the sample, there were also have the porous structures, but it has the shallow holes in that side. So after sputtering gold on this side. It also can use as one electrodes. We can use this side and the aluminum as the other capacitor which maybe have smaller capacitance than the first one. This speculation need the test result to approve. And the third one is that when we continue to expand the...
capacitance of the electrostatic supercapacitor. In the basis of high aspect ratio, we can try to increase the effective area in the other way. The parallel approach of the electrode was a well chosen based on the porous structure which we have mentioned in the design part of this article. In this process we should use ALD technology which we did not have in our lab, so I try to solve this problem in the other way. We can connect the top side and back side together and let this connected part as one electrode, and the aluminum layer between

Figure 5-2: the C-V curve of electrostatic capacitor under the different sweep rate

to increase the effective area in the other way. The parallel approach of the electrode was a well chosen based on the porous structure which we have mentioned in the design part of this article. In this process we should use ALD technology which we did not have in our lab, so I try to solve this problem in the other way. We can connect the top side and back side together and let this connected part as one electrode, and the aluminum layer between

Figure 5-3: the C-V capacitance change under the different sweep rate
them as the other electrode. These two electrodes formed a capacitor which can be equivalent to the two capacitors connect in parallel. And then test the properties of this capacitor. Find the relationship of the performance between shunt capacitor and the single one, such as the theoretical value, and loss. All of these test would provide the theoretical and data basis for future research when we fabricate capacitor in parallel connect based on AAO substrate. For the single layer supercapacitor based on AAO substrate has been published in Nature Nanotechnology 2009[5]. So for the multilayer supercapacitor based on AAO substrate can greatly increase the capacitance in this field. Therefore, this research had the great significance.

We used Zahner IM6 Electrochemical workstation to test the samples, the frequency we set 1 kHz, the voltage sweep range from 0-2V, and the sweep rate we used5mv/s, 40mv/s, 100mv/s, 200mv/s, 300m/s and 400mv/s. And then we choose two electrodes mode. In order to get a stable capacitance, the cycle we chose 3. And the sample point we chose 200. After the test we used the software of origin 8.0 to analyze the data and got the result as show in figure 5-2. From the image of the test result, under the different sweep ratio from 5mv/s to 300mv/s. All the cyclic voltammetry curve have the well rectangle characters. That means these capacitor have a very stable capacitance characteristics. It fit for using the large current and high power to charge and discharge it in a certain extent. This capacitor had the capability in using large current charge and discharge. In order to get the specific capacitance of the capacitor, we used origin 8.0 integrate the area of C-V curve under different conditions. And then used formula 5.2.5 to calculate the capacitance per square centimeter. And then also used origin 8.0 draw the figure which illustrate the capacitance change under different sweep rate. From the figure 5-3, we can see the

![Figure 5-4: the impedance change and the absolute value of phase](image)
capacitance have a significant decrease coupled with the sweep rate increase. The reason can be summed up like that there were so many porous structure in the surface of the electrode. There are also have some island structure when we use sputtering to deposit gold on the porous structure. That means somewhere of the electrode connected not very well. Under the quickly charge condition, there have not enough space and time which can used for ions go in and out. Not everywhere of the electrode layer effectively utilize. So there have a change under different scan rate.

5.1.3 Impedance test

We used Zahner IM6 Electrochemical workstation to test the impedance in AC model. And the frequency range from 0.1Hz-100kHz, and the amplitude we set 10mV. The principle of impedance test in AC model is that supplied a small amplitude AC signal on the working electrode, and test the feedback signal with complex impedance current which can used for observing the change when there have the disturbance following.

And figure 5-4 was the impedance change and the absolute value of phase. We test from the AC model. From the high frequency to low frequency the impedance have a significate decrease. That the typical characteristics of electrostatics capacitor. High frequency signal can pass the capacitor and low frequency stop here. And you also can see from the phase. In the high frequency and low frequency section, there had significant phase delay during this area. It shows obvious characteristics of capacitive reactance which delay almost 90 degree. In the midfrequency, there have obvious resistance reactance. All of these show that it have a significate capacitance characteristic.

![Figure 5-5: the cycle performance of the electrostatic capacitor](image)

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5.1.4 Cycle performance

Figure 5-5 was the cycle performance of the electrostatic capacitor based on AAO. The scan rate was 100mv/s and after 1300 cycles. At the beginning, there have only a litter change, and hundreds cycle later, there was litter change. Electric capacity of capacitor tends to be stable. And at the same time, the charging and discharging current almost symmetric. That means there have stable area for storing charge. So this electrostatic capacitor had a stable useful life and capacitive character.

5.1.5 Charge and discharge performance

When the charging current and discharge current maintain in a constant value. dU/dt also change follow the constant value. That means between electric potential and current, there have a linear relationship when they have a change. As we know

\[ \Delta U = IR \]  

(5-6)

R was the internal resistance of the capacitor, and \( \Delta U \) was the voltage drop when charge and discharge. When the current keep in a constant value, and there have linear relation between internal resistance and potential drop. From figure 5-6, we can see the voltage keep the linear change over time, so that means there have a good capacitance characteristic.
5.1.6 C-V testing on double sides AAO electrostatic capacitor

There were two sides structure about the AAO substrate. The back side of the AAO substrate also had porous structures. In order to further increase the capacitance, we deposited the Au on the back side of the AAO substrate and make a new capacitor. And

![C-V cycle test result of the top side capacitance in AAO substrate](image)

![C-V cycle test result of the bottom side capacitance in AAO substrate](image)

**Figure 5-7: (B) C-V cycle test result of the bottom side capacitance in AAO substrate**

test the capacitance compare with the top side device. There also have the other purpose which we want to get some data about the capacitors connect in parallel mode for the future research when we used ALD to make a multilayer capacitor. Because the multilayer capacitor we can connect them in parallel with the purpose of increasing the capacitance. And this experiment will compare the dissipation in real testing and theoretical value. So this testing have the important significate for will for the future of the experiment which can provides the data and theoretical support. All the test we set the scan rate of potential from -1.5V-1.5V. and the scan rate from 5mv/s to 1v/s. after test we used origin 8.0 plot all the image and integral the area. And then use formula 5. 5 to calculate the capacitance and plot the image in different conditions as show in figure 5-7.

From figure 5-7, it is very easy to find the bottom side of electrostatic capacitor have the almost same CV cycle characteristic. And it shows that the bottom sides also had the stable capacitive. In the contemplation of the design. The capacitance in bottom side is smaller than the top side because of the shallow porous structure in the bottom side. The effective
area was smaller than the top side. In the other way, it proved that the porous structure was useful in these design.

And then connected the top and back side together as an electrode and the aluminum between them as the other electrode. And these connected model equivalent to the parallel mode of two capacitor connection. All of them have the same goal which can get more effective area in the charge store. So the data we got from this sample can supply enough experience and theatrical basis for the future multilayer capacitor based on AAO substrate.

Figure 5-8 (A) is C-V cyclic test result of the two sides capacitor based on AAO substrate, we also chose the same parameters that we set in the single surface during we do the testing in the two sides model. After that compared the capacitance we got from top side, back side and parallel model, respectively. As show in figure 5.15(B). From the figure 5-8 (B) 1 you can see it very clear, the total capacitance we get from the parallel model is much bigger than the single one. And we also can get the top side capacitance was bigger than the bottom side due to the depth of the porous structure. So that means the porous structure was available for increasing the capacitance. And the blue line in image 2 was the sum of added the top capacitance and bottom capacitance. It was almost the same with the experiment value which means there almost had no dissipation. This result we got was meaningful to prove that the parallel capacitor based on AAO substrate can great increase the capacitance. So this results provided experimental basis for the further research. Figure

Figure 5-8: (B) The relationship between the single capacitor and multilayer capacitor.
Figure 5-9: The phase and impedance change under different capacitor and got the relationship between the single capacitor and multilayer capacitor.

5-9 was the ‘Bode diagram about the impedance and phase change under the different capacitor. All the capacitor have the low impedance during the low frequency. Especially when the frequency more than 10 kHz, the impedance lower than 1k. That means in all the device has the good capacitive characteristic. And in these three capacitors, the parallel mode have the lower impedance that the other, so it has the best capacitive character. That was what we want. And we also can get the character from phase diagram. During the high frequency there have good capacitive character.
5.2 Characterization of the electric double layer supercapacitors.

On the basis of the work in the previous step, prepared double layer supercapacitor based on AAO substrate. Due the limitation of instrument, in our lab we did not have ALD so we only have the sputtering in rotation mode maybe can get the better coverage ratio. I try to use sputtering to find the best parameter can get the higher coverage ratio on my porous structure which the diameter of the hexagonal only about 100 nm. In order to fully prove the porous structure was available in this design. I also fabricate one flat double layer electrode as the same dimension and the other parameters used plastic as the substrate. Figure 5-10 was the SEM image after deposit gold on the top of AAO substrate. And you can see the different between before deposition and after deposition. There had some gold grain on the top, but the AAO structures still open, have not covered by the Au layer. To make sure there have enough gold on the top of this surface. Did the component analysis by EDX as show in the figure 5-11. And also got the element composition before and after deposition in table 5.1. There have enough gold on the top of AAO substrate as electric double layer electrode. Based on the principle of electric double layer supercapacitor. Double layer capacitance $C$ was composed of inner layer capacitance $C_1$ and diffusion layer $C_2$ in series. As the
formula show in 5-7
\[
\frac{1}{C} = \frac{1}{C_1} + \frac{1}{C_2} \tag{5-7}
\]

Table 5.1 A: EDX component analysis before deposition

<table>
<thead>
<tr>
<th>Element</th>
<th>series</th>
<th>Mass wt.%</th>
<th>Norm. wt.%</th>
<th>Atom. at.%</th>
<th>Error in wt.%</th>
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<tbody>
<tr>
<td>Aluminum</td>
<td>K-series</td>
<td>28.22951</td>
<td>57.85611</td>
<td>44.87475</td>
<td>4.12229</td>
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<td>Oxygen</td>
<td>K-series</td>
<td>20.56311</td>
<td>42.14389</td>
<td>55.12525</td>
<td>7.169052</td>
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</tbody>
</table>

Table 5.1 B: EDX component analysis after deposition Au

<table>
<thead>
<tr>
<th>Element</th>
<th>series</th>
<th>Mass wt.%</th>
<th>Norm. wt.%</th>
<th>Atom. at.%</th>
<th>Error in wt.%</th>
</tr>
</thead>
<tbody>
<tr>
<td>Oxygen</td>
<td>K-series</td>
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<td>10.51591</td>
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<td>1.138323</td>
</tr>
<tr>
<td>Aluminum</td>
<td>K-series</td>
<td>24.88664</td>
<td>30.47918</td>
<td>54.14081</td>
<td>1.151045</td>
</tr>
<tr>
<td>Gold</td>
<td>M-series</td>
<td>48.17826</td>
<td>59.0049</td>
<td>14.35767</td>
<td>1.837178</td>
</tr>
</tbody>
</table>

Table 5.1 element analysis before and after deposition gold on the surface

When the electrolyte keep in low concentration, almost all the ions move to the surface fo
the electrode, fixed-layer capacitance was the major component. So C was approximately
equal capacity C1. According to the Stem model of the electric double layer. The electric
double layer on the surface of the electrode capacitance was about 20-40uF/cm² in general.
If the electrode has a larger surface area, and the capacitance was bigger. Theoretically,
AAO substrate have the larger specific surface area. So it would got bigger capacitance
than the stem model which calculate in theoretic.

Figure 5-12: three electrodes test tank

And first, we will compare the samples between flat substrate with gold layer as electrode
double layer capacitor and AAO substrate covered with gold as electrode. And we used
three electrodes no buffer model in Zahnner IM6 Electrochemical workstation. Ag/AgCl as
the reference electrode. And platinum as the counter electrode. We used sodium sulfate as
the electrolyte which the concentration was 1mol/L. The instrument as show in figure 5-12.
In order to compare the result between flat surface and porous surface of the electrode
double layer supercapacitor. We set the same parameter between these two samples. The
scan rate we used 100mv/s, the electric potential from 0-800mv and also chose the data
after 20 cycles later for the stable capacitance. Figure 5-13 was the C-V curves we got from the cyclic voltammetry. According to the energy storage principle of electric double layer supercapacitor. In the working range of the electrode. The Supercapacitor cyclic voltammetry curve should be a standard symmetrical rectangle curve, ideally. In the actual system, As a result of the electrode polarization resistance, the volt-ampere curve about the capacitance have a certain extent of deviation. From the figure 5.20 we got from origin 8.0, we can see, at the same conditions. Specific current about the porous substrate sample increased significantly compared with flat surface. So the porous structure was useful in this design. And then integral the area of the C-V curve in origin 8.0 and calculate by formula 5. 5. And capacitance was about 1.8mF/cm². That much bigger than the theoretical value which we mention in Stem model. The reason was there have a bigger specific ratio in the AAO porous structure and also had enough diameter size can let the electrolyte in and out, so in the porous structure also formed electric double layer effect. So that why we can got so big capacitance. And figure 5-14 show the C-V curves under different scan rate. From this image we can see the curves deviate from the rectangular shape which means there have big impedance in the actual capacitor. Especially under the high scan rate. Curve generally symmetrical about the point of zero. That means the redox reaction process happened on the electrode was almost reversible during the process charging and discharging. When the potential change to the direction of low potential. The current perform the characteristic of fast response. Kinetics of reversible is good during the charging and discharge program. When the potential beyond a certain range, the symmetry becomes lower. That means the capacitance of characteristic was became lower. Cycle
performance degradation. A possible reason was that the electrode disposition process did not form dense structure during the deposition process which used sputtering to deposit gold on the porous structure. When the scan rate became higher, the current increase sharply during the negative scan. Deduced there maybe have reduction reaction happen.
during this process. Because in the electric double layer supercapacitor also have the faradic supercapacitor. As show in figure 5-15 the specific capacitance was attenuated follow the scan rate increase. The main reason may be related to the adsorption. The electrolyte was the sodium sulfate aqueous solution. Adsorption and stripping about the \( \text{Na}^+ \) would happen in this cycles. After increased the scan rate, the adsorption quantity of \( \text{Na}^+ \) go in the material would decreased. Only happened on the surface. In other word, that is more adsorption occurred on the surface of the structures. Lead to specific capacitance decrease. It is demonstrated that there is a decrease in the descent velocity couple with the scanning speed increase. Because the adsorption occurred almost exclusively in the surface, the influence of the scanning rate almost negligible.

5.3 Characterization of pseudo supercapacitors based on active material of Manganese oxide

According to the principle between electric double layer supercapacitor and pseudo capacitance. There have two main difference between them:

1) In the whole process of charging, the electric double layer supercapacitor need consume electrolyte. But faradic supercapacitor did not need consume electrolyte. So the concentration of the electrolyte remained relatively stable.

2) The faradic pseudo capacitor product the capacitance across the whole electrode include the internal and external. So it can get the higher density of capacitance and energy.

At present, there have three main materials which used to fabricate electrode of supercapacitor. On is carbon materials, and the other was metallic oxide, the last was conducting polymer. And now we used manganese oxide because of this material was widely exist in nature. And the price was low, environment friendly and also have so many sulfide morphology. That the reason why we chose manganese oxide as the active material.

At present, the literature has reported so many method about the manganese oxide synthesis. Such as Liquid Phase Deposition, hydrothermal method, electro-deposition and so on. There we chose C-V cycle method to growth manganese oxide. The detail show in the part of 5.2.3. In order to prove the porous structure was useful in this design. We still prepared two types of samples. One is flat surface covered with gold, and then growth manganese oxide on the surface under same conditions compare with AAO substrate. the other was AAO substrate was covered gold on the surface and then used C-V cycle method to growth on the top of this surface.

5.3.1 SEM analysis of the material

Figure 5-16 was the SEM image about the AAO substrate before and after growth manganese oxide. A was the image only deposited gold on the top of this sample. And B was the image after growth manganese oxide. And you can see sheet like structure on the
top of the sample. That was the manganese oxide sheet. The distribution is relatively homogeneous. And there also have lumps appeared on the surface. We can see the details from image C and D, looks like transparent structure have not covered the holes of the sample. In order to check the element content. We did the component analysis used EDX. And in table 5.5 was element analysis after growth manganese oxide on the surface. There have Sodium and sulfur due to the solution we used in the growing process. For the manganese, the proportion of atoms got 13.2%. We also have the flat samples which used for getting contrast data with AAO samples. All the samples did the same process follow the AAO substrate to make sure there have the same contrast conditions. Figure 5-17 was the SEM image about the flat sample after growth manganese oxide. On the top of gold there was the manganese oxide sheet which we used C-V cycle method to grow as show in image A. And in image B was the manganese sheet after using nitrogen flow to remove some of the sheet away. And this process would let it easy to make sure where the manganese oxide was when we used mapping model to analyze the distribution. From this Image you can see clearly the very thin sheet was manganese oxide which used green to represent. Around the sheet there was gold substrate which we used red to represent. And C was the element component analysis used EDX. And we just chose the place where only had the thin sheet to test as show in the detail with enlarged scale. And D also was the

Figure 5-16 (A) was the SEM image about the AAO substrate before growth manganese oxide. Only covered with gold layer. (B) was the SEM image about the AAO substrate after growth manganese oxide. (C) and (D) were the detail with enlarged scale based on image B
Table 5-3: the element analysis after growth manganese oxide on the surface.

<table>
<thead>
<tr>
<th>Element series</th>
<th>Mass wt.%</th>
<th>Norm. wt.%</th>
<th>Atom. at.%</th>
<th>Error in wt.%</th>
</tr>
</thead>
<tbody>
<tr>
<td>Oxygen</td>
<td>K-series</td>
<td>36.88152</td>
<td>38.58394</td>
<td>64.23688</td>
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<tr>
<td>Sodium</td>
<td>K-series</td>
<td>9.627395</td>
<td>10.07179</td>
<td>11.66953</td>
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<tr>
<td>Aluminium</td>
<td>K-series</td>
<td>4.914254</td>
<td>5.141093</td>
<td>5.075399</td>
</tr>
<tr>
<td>Sulfur</td>
<td>K-series</td>
<td>4.480006</td>
<td>4.6868</td>
<td>3.893257</td>
</tr>
<tr>
<td>Manganese</td>
<td>K-series</td>
<td>26.00232</td>
<td>27.20257</td>
<td>13.1892</td>
</tr>
<tr>
<td>Gold</td>
<td>M-series</td>
<td>13.68224</td>
<td>14.3138</td>
<td>1.935727</td>
</tr>
</tbody>
</table>

Figure 5-17: A was the SEM image about the flat sample after growth manganese oxide. B was the sample after used nitrogen flow to remove some of the manganese sheet away and then do the mapping element analysis. C was use DEX to check the sheet component. D was used DEX to check the substrate component around sheet E and F were the element analysis result respond to C and D, respectively.
element component analysis used EDX. But this time we only chose the place where have no thin sheet covered in order to make sure the thin sheet was the manganese oxide. E and F was element analysis result responded to C and D respectively. So from the result we can determined there was thin sheet was the manganese oxide. And the atom content was 21.65%. The manganese content was much higher than the AAO samples. The reason was that on the flat surface the manganese have a good connect with gold and on the AAO substrate because of the porous structure the manganese connect with gold was inadequate. So the manganese on the flat surface was higher than the porous structure.

5.3.2 C-V testing on the pseudo supercapacitor

A. Compare the specific capacity between flat substrate with gold and flat substrate with gold and manganese oxide. Figure 5-18 was the C-V images of the flat substrate. We also used three electrode test method to test these samples. Using 1 mol/L sodium sulfate solution as electrolyte. And Ag/AgCl as the reference electrode. platinum as the counter electrode. The scan rate we chose 100mv/s and the potential range used 0-0.8v. In order to get the stable data, we chose the data after three cycles later and then used origin 8.0 to draw the image. From this figure you can see the difference was clear. The red one was the flat substrate with manganese oxide. And the black curve was the flat substrate just coated with gold as the double layer electrodes. The area of the curve about the flat substrate with manganese oxide was much bigger than the sample only have gold on top. This illustrated the pseudo supercapacitor was much bigger than electric double layer supercapacitor. So from this figure we got conclusion the manganese we grew by this method was available.

Figure 5-18: the C-V images about the flat substrate covered different material
B. Compare the specific capacity between AAO substrate with gold and AAO substrate with gold and manganese oxide. Figure 2-19 was the C-V images about the AAO substrate.

We also used three electrode no buffer test model to test these samples. Using 1mol/L sodium sulfate solution as electrolyte. And Ag/AgCl as the reference electrode. Platinum as the counter electrode. The scan rate we also chose 100mv/s and the potential range used 0-0.8v. In order to get the stable data, we chose the data after three cycles later and then used origin 8.0 to draw the image. All the parameters we chose here with the purpose of comparing the result more easy. From this figure you can see the difference was clear between AAO substrate only covered with gold and manganese oxide. The red curve had much bigger current change and area during the measurement. The specific capacity of pseudo capacitor was much bigger than the electric double layer capacitor. The active material we made by C-V cycle can greatly increase the specific capacitance. There also have no obvious redox peak. That means the material have good electrochemical reversibility.

C. Compare the specific capacity between flat substrate with manganese oxide and AAO substrate with manganese oxide. Figure 5-20 was the C-V images based on AAO substrate and flat substrate. We also used three electrode no buffer test model to test these samples. Using 1mol/L sodium sulfate solution as electrolyte. And Ag/AgCl as the reference electrode. Platinum as the counter electrode. The scan rate we also chose 100mv/s and the potential range used 0-0.8v. In order to get the stable data, we chose the data after three cycles later and then used origin 8.0 to draw the image. All the parameters we chose here with the purpose of comparing the result more easy. From this figure you can see the
difference was clear between AAO substrate with manganese oxide and flat substrate with manganese and oxide. We had used EDX to test the component analysis about manganese. The atom content in flat was 21% and in AAO substrate was 13%. The content was a little more than AAO substrate. But the area under the red curve was much bigger than the black one. That illustrated the specific capacity of flat substrate was much smaller than the AAO substrate. This specific capacity difference was made by the microstructure of the electrode. On the top of AAO substrate have so many porous structure which can greatly improve the specific surface area. So there have more active sites during the electrochemical reaction in electrolyte. Therefore, increasing the specific capacitance of this material. And then we used origin 8.0 integral the area and used formula (5-5) to calculate the specific capacitance square centimeter. And the result was 47.1mF/cm². There also have no obvious redox peak. That means the material have good electrochemical reversibility. So from this image we get that the porous structure on the substrate was quite useful to improve the capacitance. And use AAO structure as the substrate to fabricate the supercapacitor electrode have a good prospect.

D. Cyclic voltammetry for a MnO2 AAO electrode cell in mild aqueous electrolyte. Figure 5-21 was the schematic of cyclic voltammetry for a MnO2 electrode cell in mild aqueous electrolyte (1.0mol/L Na2SO4). And the potential range from 0v-0.8v. The curves describe the specific change under different scan rate. When the scan rate over 20mv/s, and the curves deviated from the rectangular. The capacitance deviated from electric double layer supercapacitor. The properties of the specific capacity would be deteriorated with the increase of scan rate. The reason was that we have used sputtering to deposit gold on the top of AAO substrate as the electrode. But this process was not the conformal process. So
the continuity of membrane was not good. The electrical conductivity must be decreased. So the shape deviated from rectangular. There have no obvious redox peak. The reason was the electrochemical reaction is continuous and the material have good electrochemical reversibility [333]. There are many possible reasons for this. The manganese had the high dispersion. The manganese had the good contact with gold. The aperture of the porous structure was easy to go through and out during the reaction. So from all the result we get that if we use AAO as the substrate to make electrode can greatly increase the specific area and specific capacity. But there also have some point we can improve, for example. For getting the high density, continuity and conformal electrode film to increase the electrical

Figure 5-21: The schematic of cyclic voltammetry for a MnO₂ electrode based on AAO substrate
conductivity and aspect ratio. ALD process was a better choice than sputtering. So in the future research we can use ALD instead of Sputtering to deposit the electrode layer.

E. Cyclic voltammetry for the second time deposited MnO$_2$ on the AAO substrate. Figure 5-22 was the cyclic voltammetry for the first time and second time deposited MnO$_2$ on the AAO substrate. And the scan rate here we chose 100mv/s. and potential range from 0V to 8V. After the first time we deposited the manganese on the substrate. And then after testing, in order to check if there have more manganese oxide on top of the surface, maybe will get

![Image of cyclic voltammetry](image)

Figure 5-22: Cyclic voltammetry for the first and second time deposited MnO$_2$ on the AAO substrate.

![Image of AAO surface topography](image)

Figure 5-23: the AAO surface topography after second deposition manganese oxide
more high specific capacity. So did the same process for deposition manganese oxide as the first time. But this time only chose 10 cycles. In figure 5.29, the blue curve was the C-V curves after second deposition. The red one was result after the first deposition. And there have an obvious decrease about the specific capacitance. It was not in accordance with our inference. So in order to find the reason, we used SEM to check. Figure 5-23 was the AAO surface topography after second deposition manganese oxide. Too much manganese oxide would form plates or plate like objects on the top of porous structure. And this plate like object would cover the porous structure and decreased the specific area during the reaction. The electrolyte was difficult to go in and out of the nano-holes during the reaction process. So from this result we also can get that the nano-holes on the AAO substrate was useful for store energy.

5.4 Conclusions

The AAO nano template at both side of aluminum substrate was successfully fabricated by two-step anodic oxidation. The morphology and structure of the AAO nano template was characterized by SEM and AFM. We find that the nano dimensions of AAO strongly depends on the electrochemical etching parameters, such as, voltage and time. The thesis has reported the fitting equations for the AAO thickness and nano aperture size versus the etching voltage and etching time. By process optimization, we are able to improve the processing speed and controlling demanded nano features used as electrode scaffold of supercapacitors.

Using the AAO nano template, by sputtering or ALD deposition of metal and dielectric layers in sequence we have designed multilayer electrostatic capacitor configuration. According different deposition techniques, e.g., sputtering or ALD, the different processing flow was designed for fabrication electrostatic ultracapacitors. The device of proof of the concept has been processed on the plenary substrate. The experiment result was not as expected due to the in house sputtering technology for this application was not optimized. However, the design and fabrication laid a foundation for the future research.

AAO nano template as the electrode scaffold, by depositing gold layer as the current collector and active electrode we have fabricated the electrochemical double layer supercapacitors. Loading MnO2 on the gold layer by CV cycle method, we also fabricated pseudo supercapacitors. It proves that the CV cycle method was an effective technique to grow MnO2 on the AAO nano template. Zahner IM6 Electrochemical workstation were utilized to characterize the supercapacitors performance. The specific capacitance of electrochemical double layer supercapacitor was about 1-10mF/cm2. The specific capacitance of pseudo supercapacitor was about 50-100mF/cm2.
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