Wafer-Level Packaged MEMS Switch with TSV

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Outline

Introduction
- MEMS acceleration switch
- Through-silicon vias
- Wafer-level packaging

Fabrication
- Through-silicon vias
- MEMS switches
- Wafer-level encapsulation
- Direct mounting on PCB

Characterization
- TSVs
- MEMS switches

Summary
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MEMS acceleration switch

- **Definition**: a device that closes (or opens) a circuit above a certain acceleration threshold

- **Types**: intermittent or persistent

- **Presented application**: safety and arming devices (SADs) in smart ammunition fuzes

- **Environmental conditions**:
  - Setback acceleration pulse > 60 000 g, centripetal acceleration up to 9 000 g/mm
  - Severe shock and vibrations
  - Severe climatic conditions (e.g. -54°C to +71°C)
MEMS acceleration switch

- Why MEMS?
  - Reduced size
  - Low cost

- Presented switch:
  - Intermittent switch
  - Centripetal acceleration threshold: 13 800 g (designed)
  - Operation: freestanding structure moves in lateral plane and makes contact with neighboring structure
  - Trenches in device layer used to isolate different parts
Through Silicon Vias

- **Main motivation**: miniaturization

- **TSV in device wafer**:
  - No electrical interconnect required between cap and device wafer
  - Visual inspection still possible after flip-chip mounting (if glass cap)
  - Via-first approach must be used
Wafer-level packaging

- Why WLP ?
  - Reduced packaging costs
  - Protection of fragile MEMS structures during wafer dicing

- Presented method :
  - Adhesive wafer bonding with BCB :
    → robust, low-cost, CMOS compatible
    → protects structures from liquids, particles and dust
      (but not fully hermetic)
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Through Silicon Vias

- **Via etch**:  
  - SOI substrates (100 mm)  
  - 7 x 70 µm trenches  
  - Bosch DRIE process  
  - Al etch mask and etch stop

- **Via filling**:  
  - Thermal oxidation (1 µm)  
  - LPCVD undoped polysilicon  
  - Phosphorous gas phase doping (POCl₃)

- **Etchback**:  
  - Removal excess polysilicon
Through Silicon Vias

- **Main challenges:**
  - High aspect ratio DRIE
  - BOX etch at the bottom of narrow trenches
  - Conformal polysilicon filling

- **Results:**
  - Multi-step etch recipe with excellent profile and AR 50:1
  - BOX etch recipe with LF bias
  - Seam left in the center but sealed at the wafer surfaces
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MEMS switches

- **Protection TSV sidewalls**
  - Stripping SiO₂ frontside
  - 100 nm poly deposition

- **DRIE device layer**:
  - 2.6 µm HiPR6517 photoresist mask

- **Release movable structures**:
  - 1 hr HF vapor release at 35°C

- **Au metallization**:
  - RIE 100 nm polySi
  - NiCr barrier/adhesion layer
  - 500 nm Au sputtering
MEMS switches

- **Main challenges:**
  - Vertical profile DRIE
  - Planarity of released structures after metallization

- **Results:**
  - DRIE process with vertical sidewalls and small scallops
  - Slight (< 1 μm) upwards bending of cantilever structures
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**Wafer-level encapsulation**

- **Etch cavities in glass wafer:**
  - TiW/Au etch mask
  - Wet etch of glass (49 % HF at room temp)
  - Etch depth: 20 µm
  - Stripping of TiW/Au

- **BCB coating glass cap wafers:**
  - Cyclotene 3022-35 (BCB)
  - Spray coating with airbrush pressurized with dry N₂
  - 1.4 µm thickness
  - Hotplate 90 sec 110 °C
Wafer-level encapsulation

- **Wafer bonding**:
  - Suss BA6 bond aligner
  - Suss SB6 thermo-compression bonder
  - Pre-heating 5 min 150 °C
  - Pressure: 300 mbar
  - 1 hr 250 °C

- **Patterning backside metal**:
  - AZ4562 photoresist mask
  - Wet etching of NiCr/Au

- **Dicing with conventional diamond saw**
Wafer-level encapsulation

- **Main challenges:**
  - Particles and defects
  - BCB reflow within the cavity

- **Results:**
  - Successful bond over the complete wafer
  - Particles and defects embedded in bond seal
  - Acceptable reflow
  - Efficient sealing/protection during dicing
Wafer-level encapsulation

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Direct mounting on PCB

- **Mounting of chips**:
  - Direct on FR-4 PCB
  - Novel isotropic conductive adhesive (ICA) with uniform Ag-coated polymer spheres
  - Dima HS-100 stencil printer
  - MyData My-9 pick and place
  - Curing 60 sec 150 ºC
  - Pad size: 250 x 440 µm
  - Pad pitch: 600 µm
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Characterization of TSVs

- **Results**:  
  - Via resistance ~ 4.5 Ω  
  - High yield also for daisy chains with 180 vias
Characterization of switches

- **Test system:**
  - FR-4 PCB with two MEMS chips
  - Test PCB with data logger
  - Placed in sample holder for centrifuge and filled with a powder consisting of 40 to 80 µm glass beads
  - Sorvall WX80 Ultra centrifuge

Ø 20 x 35 mm test system
Characterization of switches

- Results:
  - Closing threshold ~ 11 800 g (15 % lower than expected)
  - Opening threshold ~ 10 500 g (some stiction)
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- Polysilicon TSVs with 4.5 Ohm/via were successfully fabricated through 340 µm thick SOI wafers.

- A new RIE process based on LF substrate bias was successfully developed to etch a 2 µm BOX layer at the bottom of high aspect ratio ratio trenches.

- A simple and robust method for wafer-level encapsulation with non-photosensitive BCB adhesive was demonstrated.

- Direct mounting of MEMS devices onto a PCB using a novel isotropic conductive adhesive was demonstrated.

- A miniaturized wafer-level packaged MEMS acceleration switch with TSVs was successfully fabricated.
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