3D Interconnect Technologies For Advanced MEMS/NEMS applications

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Outline

- 3D Integration
  - Motivation
  - Evolution
  - Key processes

- 3D Integration of MEMS/NEMS and IC
  - More than Moore
  - Key market driver
  - Specific challenges for MEMS/NEMS

- 3D Technologies for integration of MEMS/NEMS and IC
  - TSVs for MEMS
  - Bonding of MEMS and IC

- Technology demonstrators

- Summary
3D integration

Motivation
- Miniaturization
- Increased interconnect speed
- Reduced RC delays
- Reduced power consumption
- Reduced overall costs
- Increased yield and reliability
- Reduced weight
- Increased functionality

Evolution
- Multi chip modules (not 3D)
- 3D packaging: chip scale stacking without through silicon vias
- 3D integration: through silicon vias (TSV), wafer level bonding
3D integration

Key processes

- Through silicon/substrate vias (TSVs)
  - Electrical interconnects through the chips

- Bonding
  - Mechanical and electrical interconnection between the chips in the IC stack
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3D integration of MEMS/NEMS and IC

More than Moore

- Moore’s Law scaling alone can not maintain the progress of smart systems → heterogeneous integration

More Moore: Scaling

Baseline CMOS: CPU, Memory, Logic

More than Moore: Functional Diversification

Source: Dr. Peter Ramm
Fraunhofer IZM Munich
3D integration of MEMS/NEMS and IC

- Key market driver: portable consumer electronics
  - Cell phones, PDAs, laptops, game controllers (e.g. Nintendo Wii, PS3), etc
  - New functionality based on MEMS: drop detection, motion sensor, etc
  - Requirements: small size, low cost, low power

Kionix, KXPB5
3-axis accelerometer

ST Microelectronics, LIS331DL
3-axis accelerometer

Sonion, DigiSiMic
digital MEMS microphone

Source: Chipworks
3D integration of MEMS/NEMS and IC

- Specific challenges for MEMS and NEMS
  - Substrate thickness (300 to 1000 µm)
    - MEMS structures rely on a certain mass/volume/thickness for stability/reliability/strength: the substrate cannot be thinned
    - High aspect ratio etch is difficult -> trade-off thickness vs via pitch
  - Substrate material
    - Anodic bonding of glass-to-silicon wafers is commonly used for reliable hermetic sealing of MEMS -> DRIE not possible
    - MEMS or often fabricated on SOI wafers -> complicates DRIE
  - Wet processing for devices with inlets/released structures
    - Wet etching and cleaning, electroplating, etc can be problematic when inlets or released structures are present
  - High topography
    - MEMS devices often have high topography surfaces (e.g. inlets or movable parts) which can be a challenge for the processing
  - Functional and nano materials with temperature limitations
    - e.g. organic coatings on optical sensors
  - Fragility of MEMS/NEMS structures
    - Might not allow certain processes
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TSVs for MEMS vs IC

IC → many interconnection points:
   - small pitch required
   - achieved by thinning the substrates

MEMS → typically fewer interconnection points:
   - substrate cannot be thinned
   - trade-off between pitch and thickness
   - high aspect ratio vias
Au vias through anisotropically wet-etched Si cap wafers

HyCap®
- Anisotropically wet etched vias in Si wafer (KOH)
- No DRIE
- Electroplated Au metallization

www.hymite.com
Bulk Si TSVs isolated by a dielectric trench Silex

- Bulk Si TSVs
  - Via first approach
  - DRIE trenches in low resistivity wafer filled with SiO₂
  - allows high temperature post processing
  - sub 50 µm min pitch for 300 to 600 µm thick Si wafers

- Metal vias with Au or Cu for RF MEMS (< 50 mOhm/via)

www.silexmicrosystems.com
Hollow and filled polySi TSVs
SINTEF

- Via first approach
- allows high temperature post processing
- Dry-film resist for patterning of hollow vias
- TSV technology platform for MEMS and interposers being established

Min pitch vs substrate thickness

![Graph showing min pitch vs substrate thickness for hollow and filled TSVs.](image)

- Hollow TSVs expected from DRIE results
- Demonstrated filled TSVs
- Development ongoing

- 50 µm scale bar

Nicolas Lietaer, SINTEF ICT
Hollow and filled polySi TSVs for SOI wafers

- polySi TSVs for SOI wafers under development
  - DRIE 5 µm wide structures through 20 and 43 µm SOI layer ✓
  - BOX oxide etch development ✓
  - DRIE development ongoing
Glass wafers with bulk silicon vias

Planoptik

- Silicon glass compound wafers
- Hermetic vias and hermetic seal to sensor wafer
- Visual inspection possible
- Large design freedom

Source: SensoNor

Source: SINTEF/Planoptik

Source: SINTEF
Glass wafers with tungsten vias
NEC Schott

- HermeS™
  - Tungsten TSVs in glass wafers
  - Hermetic vias and hermetic seal to sensor wafer
  - Visual inspection possible
  - 300 µm min pitch for 500 to 600 µm thick glass wafers

Technology details of HermeS™ Glass substrate solution (Courtesy of NEC Schott)
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Bonding of MEMS/NEMS and IC

- Selection criteria for bonding technology
  - Chip-to-wafer or Wafer-to-wafer
  - Interconnection pitch
  - Number of I/O
  - Dry/wet processing
  - Alignment accuracy
  - Stand-off height
  - Hermeticity
  - Reliability
  - Cost

- Required: electrical and mechanical interconnection
Bonding of MEMS/NEMS and IC

- **Chip-to-wafer bonding**
  - Wafer size and chip size mismatch between MEMS and IC is not an issue
  - Known good dies: lower yield of MEMS devices is not an issue

- **Wafer-to-wafer bonding**
  - Simpler process
  - More cost-effective (?)
  - Better alignment accuracy
  - Smaller min pitch

- **Bump technologies: from solder balls to SLID**

  - **Conventional solder balls** (solder paste screen printing)
    - min pitch ~ 150 µm
    - min stand-off ~ 80 µm

  - **Au stud bumps**
    - min pitch ~ 70 µm
    - min stand-off ~ 10 µm

  - **Jetted microbumps**
    - min pitch ~ 80 µm
    - min stand-off ~ 60 µm

  - **Plated solder microbumps**
    - min pitch ~ 25-50 µm
    - min stand-off ~ 25 µm

  - **CuSn SLID**
    - min pitch ~ 10 µm
    - min stand-off ~ 10 µm
Au stud bump bonding

- Chip to wafer
- Min pitch ~ 70 µm
- Stand-off height: ~ 10 - 20 µm
- No wet processing involved
- No need for UBM or passivation layers
- Most cost-effective for devices with lower I/O counts
- Demonstrated for stacking of MEMS onto ASIC (incl. reliability)

Source: Kulicke & Soffa

Source: SINTEF

N. Lietaer, iMAPS Int Device Packaging Conf, 2009
Plated solder microbumps

Example: SnAg

- Chip to wafer
- Min pitch 35-50 µm
- Stand-off height: < 30 µm
- Misalignment < 2 µm
- Passed extensive reliability tests

Reliability tests
- 1000 cycles ÷ 40 – 150 °C
- 260°C 30 min
- 100% humidity, 121°C, 2 bar
- Electromigration
- High temperature storage

Source: SINTEF/Fraunhofer IZM Berlin

Cu/Sn Solid-Liquid InterDiffusion (SLID)

- Chip to wafer
- Min pitch of 10 to 60 µm
- Stand-off height : ~ 10 µm
- Connection points : 5 x 5 µm to 30 x 30 µm

Process:
- During bonding at 325°C, Sn melts
- Cu diffuses into the melted Sn layer to form Cu$_6$Sn$_5$ (η) → the compound solidifies and the stack is fixed
- Cu$_6$Sn$_5$ (η) then transforms into the thermodynamically stable Cu$_3$Sn (ε) phase with melting point > 600°C

Source: SINTEF / FhG IZM

R. Wieland, RTI conference, 2005
Anisotropic conductive adhesives/films (ACA/ACF)

- Chip to wafer
- Min pitch < 100 µm
- Stand-off height < 10 µm
- Temperature: 150 – 200 ºC without custom-tailoring
- Feasibility study for MEMS/IC applications
  - ACF with 5 µm Ø Ni/Au coated polymer spheres bonded at 180ºC, 30s, varying pressure

100 MPa (low range of pressure)

120 MPa (optimised process)

140 MPa (too much pressure)

160 MPa (too much pressure)

suitable deformation

Nguyen, IMAPS Nordic, 2009
Metal thermocompression bonding

- Cu, Au, Al
- Objective: recrystallisation
- Temperature, pressure, time

K.N. Chen, Elchem Sol State Letters, 2004
Metal thermocompression bonding
Example: Tezzaron Cu-Cu

- Chip to wafer
  - Min pitch 25 µm
  - 10 x 10 µm bond points

- Wafer to wafer
  - Min pitch 2.4 µm
  - 1.7 x 1.7 µm bond points
  - Bond temperature 400°C
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e-CUBES automotive demonstrator

- Automotive demonstrator: miniaturized Tire Pressure Monitoring System (TPMS)

Today’s TPMS

- Rim based TPMS
- Pressure inlet hole
- Interchip bonding
- ASIC

Source: SensoNor

3D integrated TPMS

- < 1 cm³

N. Lietaer, iMAPS Int Device Packaging Conf, 2009
TPMS building blocks

- MEMS Pressure sensor
- TX – sensor interconnect
- Transceiver ASIC
- μController ASIC
- μC – TX interconnect
- Sensor TSVs
- MEMS Bulk acoustic resonator
- TX TSVs
- TX – BAR interconnect
Technology choices

- **Au stud bumps with adhesive**
- **SnAg microbumps and underfiller**
- **Silicon-glass compound wafer with TSVs (alternative: hollow TSVs)**
- **TSV with W**
- **Au stud bumps only**

Sources:
- SINTEF/FhG IZM-Berlin
- Kulicke & Soffa
- Fraunhofer IZM-Munich
- SINTEF/SensoNor/PlanOptik
EU project DAVID

DAVID: Downscaled Assembly of Vertically Interconnected Devices
- provide extremely high packaging density for hybrid integration of MEMS with ASICs

Main technologies
- Post CMOS TSVs in ASIC
- Au-Sn bonding for the mechanical, hermetic and electrical joining of MEMS and ASIC
- Fine pitch solder balling

Total package height < 1 mm

http://www.david-project.eu/
VTI technologies Chip-on-MEMS

- Chip-to-wafer
- Thinned ASIC IC flip-chipped to MEMS wafer with solder bumps
- Known good die
- Total height < 1 mm
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Summary

- There is an emerging market for 3D Integration of MEMS/NEMS and IC

- A number of challenges need to be addressed for fabricating TSVs through MEMS/NEMS structures, but solutions are being developed and demonstrated

- Metal bonding technologies used/developed for packaging and 3D integration of conventional ICs will also be applicable for 3D integration of MEMS/NEMS and IC

- Today, differences in wafer size, die size and yield make chip-to-wafer bonding the preferred approach for stacking of MEMS/NEMS and IC