Acoustic/Electronic stack design, interconnect, and assembly
Techniques available and under development

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MI-lab Work-shop on future ultrasound probe technology
Trondheim, March 26. 2009
Outline

- 3D integration of MEMS/IC
- Solutions for through silicon vias
- Solutions for interconnects
- Examples of applied technologies
- Coming project
- Summary
MEMS: Micro electromechanical systems

- Enables
  - Sensors
  - Actuators
    - cMUT: Both

- Demands
  - “Window” to the environment
  - ASICs for calibration and control
    - cMUT: Logic and memory

Source: www.ece.cmu.edu/~dwg/research/ae.html
Existing packaging solutions

Market driver examples
- Nintendo Wii
- Mobile phones

The progress
- Side by side, wire bonded
- 3D stacked with wire bonds
- Integrated in-plane
- Interposer with through silicon vias (TSVs)
- Wafer level packaging…

Source: CHIPWORKS
Wafer level packaging (WLP)

- No wire bonds
  - Through Silicon Vias (TSVs) required
  - Interconnects defined on wafer level
- Ready for surface mounting after final dicing

Source: VTI
cMUTS: MEMS wafer TSVs / interposer

Surface micromachining or based on bonding

Interposer

RDL

TSV technology choice

Pitch: 25 µm
Wafer thickness: 30-100 µm
Aspect ratio: 10-20
TSVs

Pitch <50 µm, wafers <100 µm (ICs)

Source: Tezzaron

Source: ZyCube

Source: Honda

Poly Si, W, Cu, conductive paste

Source: Fraunhofer IZM-Munich
Definitions of TSVs

- Front-end-of-line (FEOL)
  - Before IC wiring
- Back-end-of-line (BEOL)
  - During IC wiring in IC foundry
- Post-BEOL
  - Following complete IC fabrication
- Vias First
  - Made before wafer bonding
- Vias Last
  - Made after wafer bonding and thinning

*Handbook of 3D Integration (Garrou, Bower and Ramm)*

Source: Fraunhofer IZM
TSVs

Pitch >50 µm, wafers >100 µm (MEMS)

Si pins in Si

Hollow vias in Si

www.silex.com

Source: SINTEF
Interconnects
Pitch <50 µm, stand-off height ~5 µm

In/Au, Cu, Ni

Source: Ziptronix

Source: ZyCube

Source: Tezzaron

Source: Ziptronix
Interconnects
Pitch >50 µm, stand-off height ~10-20 µm

Au stud bump bonding (SBB)

SnAg/AuSn microbumps

Source: SINTEF/Datacon

Cu/Sn SLID

Au, Cu/Sn, SnAg, AuSn

Source: SINTEF/Fraunhofer IZM-Munich

Source: SINTEF/Fraunhofer IZM-Berlin
Examples using 3D stacking technologies

Lesson learned from nature about 3D stacking

Moss, flexible by thinning

High aspect ratio pillars on a leaf

Source: MEMS-Point, Thomas Brunschwiler
3D integrated planar silicon sensor

- Fingerprint sensor
  - Navigation and pointer detection
  - TSVs through sensor
    - Pitch 50 µm
    - 20 µm wide
  - Bumps for interconnect
    - Routed out

Technology demonstrator

- Hollow vias with gold stud bumps (HoViGo)
  - High yield
  - Good reliability

Pitch: 110 µm
Stand-off height: 10-15 µm

Source: SINTEF
e-CUBES TPMS demonstrator

- Develop wireless sensor networks with miniaturized sensor nodes
- 3 demonstrators
  - Health and fitness
  - Aeronautics and space
- Automotive
  - Tire Pressure Monitoring System (TPMS)

20 cm³

<1 cm³

in 5 years from now: e-CUBES-type Tire Pressure Monitoring System

Maaike Taklo, SINTEF IKT
TPMS building blocks

- µ-controller ASIC (µC) : 4.3 x 3.8 mm²
- Transceiver ASIC (TX): 3.8 x 3.3 mm²
- MEMS pressure sensor: 1.8 x 2.1 mm²
- MEMS bulk acoustic resonator (BAR): 0.8 x 1.3 mm²
  - Antenna, battery, outer package
Technology choices

- Au stud bumps with adhesive (alternative: SLID)

- SnAg microbumps and underfiller

- TSV with W

- Silicon-glass compound wafer with TSVs (alternative: hollow TSVs)

- Au stud bumps only (alternative: SLID)

Sources:
- SINTEF
- FhG IZM- Berlin
- Kulicke & Soffa
- Fraunhofer IZM-Munich
- SINTEF/ SensoNor/ PlanOptik
TPMS demonstrator results

- Successful measurements on PCB level
  - Communication with TX
  - Communication with μC
  - BAR is running at correct frequency

- Sensor performance to be measured soon
ReMi (KMB, BIA)

- Fine Pitch Interconnect of Microelectronics and Microsystems for use in Rough Environments
- 3 case studies
  - New or significantly improved devices for challenging environment applications
- SINTEF, VUC, FFI
- 6 Norwegian companies

Comparison commercial adhesive and silver coated spheres

Metal coated polymer spheres (ICA/ACA/ACF)

Source: Conpart
Coming:

- ENIAC
- SUB-PROGRAMME 8
  - Equipment & Materials for Nanoelectronics
- 20 partners
  - SUSS, FCI, FhG, LETI, Infineon, ALES, ASM…etc
- Kick-off: 2009-04-07
Summary

- A number of 3D stacking technologies are emerging
- Technology choice depends on required
  - Pitch
  - Aspect ratio
  - Stand-off height
  - Number of I/O counts
  - Compatibility of wafer/processes
- Research has come quite far, large activity
  - www.3dic-conf.org
- Industry coming
  - Optical devices
  - MEMS
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